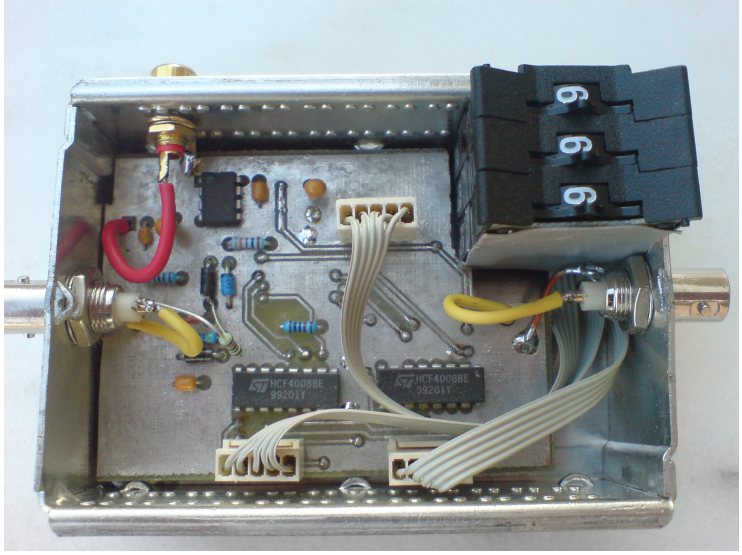
ΤΕΧΝΟΛΟΓΙΚΟ ΕΚΠΑΙΔΕΥΤΙΚΟ ΙΔΡΥΜΑ ΚΡΗΤΗΣ

ΤΜΗΜΑ ΗΛΕΚΤΡΟΛΟΓΙΑΣ

ΠΤΥΧΙΑΚΗ ΕΡΓΑΣΙΑ



ΘΕΜΑ : ΣΧΕΔΙΑΣΗ ΚΑΙ ΚΑΤΑΣΚΕΥΗ ΜΟΝΑΔΟΣ ΚΑΘΥΣΤΕΡΗΣΗΣ ΠΑΛΜΩΝ ΤΑΣΕΩΝ TTL ΜΕ ΔΙΑΚΡΙΤΙΚΗ ΙΚΑΝΟΤΗΤΑ ΤΗΣ ΤΑΞΕΩΣ ΤΟΥ ΝΑΝΟΔΕΥΤΕΡΟΛΕΠΤΟΥ

Εισηγητής : Ταταράκης Μιχάλης

Επιμέλεια : Δρουδάκης Γρηγόρης

ΗΡΑΚΛΕΙΟ, 08-06-2010

ΕΥΧΑΡΙΣΤΙΕΣ

Θα ήθελα να ευχαριστήσω θερμά τον εισηγητή μου Δρ. Ταταράκη Μιχάλη για τις υποδείξεις του και την βοήθεια του στην αποπεράτωση της πτυχιακής εργασίας. Τον Καθηγητή Δρ. Ιωάννη Χατζάκη για την καθοριστική συμβολή του στην κατασκευή της μονάδας καθυστέρησης καθώς και τον ερευνητή Δρ S. M. Hassan για την βοήθεια του στην πραγματοποίηση των πειραματικών μετρήσεων στο εργαστήριο Οπτοηλεκτρονικής, Laser & Τεχνολογιών Πλάσματος του Τμήματος Ηλεκτρονικής στα Χανιά.

Στον ανηψιό μου Δρουδάκη Γ. Μάρκο

ΠΕΡΙΛΗΨΗ ΠΤΥΧΙΑΚΗΣ

Στα πλαίσια αυτής της εργασίας σχεδιάστηκε και κατασκευάστηκε μια μονάδα χρονικής καθυστέρησης παλμών TTL με βήμα 1nsec και μέγιστη καθυστέρηση περίπου 1μsec. Η υλοποίηση στηρίχτηκε σε ειδικά ολοκληρωμένα κυκλώματα που κατασκευάζονται για να υλοποιούν χρονοκαθυστερήσεις. Το τελικό αποτέλεσμα είναι ένα κύκλωμα καθυστέρησης χρόνου παλμών, ικανό να παράγει προγραμματιζόμενες χρονοκαθυστερήσεις ειδικά σχεδιασμένο και κατασκευασμένο για λειτουργία σε περιβάλλον με υψηλό θόρυβο.

ΠΕΡΙΕΧΟΜΕΝΑ

ΚΕΦΑΛΑΙΟ 1

ΕΙΣΑΓΩΓΗ

Ένα σύστημα του οποίου το σήμα εξόδου είναι καθυστερημένο κατά ένα καθορισμένο χρονικό διάστημα σε σχέση με το σήμα εισόδου του ονομάζεται κύκλωμα καθυστέρησης χρόνου. Στις πρώτες μορφές των κυκλωμάτων καθυστέρησης οι πληροφορίες εισάγονταν με τη μορφή ηλεκτρικών σημάτων και μετατρέπονταν σε μηχανικά κύματα που μεταδίδονταν σχετικά αργά σε ένα μέσο, όπως ένα κύλινδρο γεμάτο με υγρό, υδράργυρο, μαγνητικό πηνίο, ή πιεζοηλεκτρικό κρύσταλλο. Μόλις, τα κύματα, έφταναν στο άλλο άκρο του μέσου μετάδοσης, μετατρέπονταν και πάλι σε ηλεκτρικά σήματα, καθυστερημένα κατά το χρόνο μετάδοσής τους στο μέσο. Σήμερα υπάρχουν ειδικά ολοκληρωμένα κυκλώματα που κατασκευάζονται ειδικά για να υλοποιούν χρονοκαθυστερήσεις. Η συγκεκριμένη εργασία περιγράφει ένα κύκλωμα καθυστέρησης χρόνου παλμών, στηριγμένο σε τέτοια ολοκληρωμένα κυκλώματα, ειδικά σχεδιασμένο και κατασκευασμένο για λειτουργία σε περιβάλλον με υψηλό θόρυβο και παράγει προγραμματιζόμενες χρονοκαθυστερήσεις.

ΑΝΤΙΚΕΙΜΕΝΟ ΤΗΣ ΕΡΓΑΣΙΑΣ

Στην συγκεκριμένη πτυχιακή εργασία σχεδιάστηκε και κατασκευάστηκε μία μονάδα καθυστέρησης παλμών τάσεως TTL διακριτικής ικανότητας του νανοδευτερολέπτου. Ακόμα πραγματοποιήθηκαν πειραματικές μετρήσεις στο εργαστήριο Οπτοηλεκτρονικής, Laser & Τεχνολογιών Πλάσματος του Τμήματος Ηλεκτρονικής στα Χανιά οι οποίες και παρουσιάζονται στη συνέχει αυτής της εργασίας.

ΣΚΟΠΟΣ ΤΗΣ ΕΡΓΑΣΙΑΣ

Σκοπός της παρούσας πτυχιακής εργασίας είναι η εύρεση του καλύτερου δυνατού τρόπου για να πετύχουμε καθυστέρηση της τάξεως του νανοδευτερολέπτου ηλεκτρονικά.

ΔΙΑΡΘΡΩΣΗ ΤΗΣ ΔΙΠΛΩΜΑΤΙΚΗΣ

Η διπλωματική εργασία αποτελείται από 5 ακόμα κεφάλαια η διάρθρωση των οποίων έχει ως ακολούθως. Στο Κεφάλαιο 2 παρατίθενται μία ιστορική αναδρομή σχετικά με το πως δημιουργήθηκε η ανάγκη για τα συστήματα καθυστερήσεων (delay lines). Στο Κεφάλαιο 3 γίνεται αναφορά για ορισμένους από τους τρόπους που μπορούμε να επιτύχουμε χρονική καθυστέρηση στα ηλεκτρονικά. Στο Κεφάλαιο 4 γίνεται περιγραφή της μονάδας που κατασκευάσαμε ενώ στο Κεφάλαιο 5 παρουσιάζονται οι εργαστηριακές μετρήσεις που πραγματοποιήθηκαν στο εργαστήριο Οπτοηλεκτρονικής, Laser & Τεχνολογιών Πλάσματος του Τμήματος Ηλεκτρονικής του ΤΕΙ Κρήτης στα Χανιά και αναφέρονται τα συμπεράσματά μας.

ΚΕΦΑΛΑΙΟ 2

ΙΣΤΟΡΙΚΗ ΑΝΑΔΡΟΜΗ[5]

Ένα σύστημα του οποίου το σήμα εξόδου είναι καθυστερημένο κατά ένα καθορισμένο χρονικό διάστημα σε σχέση με το σήμα εισόδου του ονομάζεται κύκλωμα καθυστέρησης χρόνου. Στις πρώτες μορφές των κυκλωμάτων καθυστέρησης, οι πληροφορίες εισάγονταν με τη μορφή ηλεκτρικών σημάτων και μετατρέπονταν σε μηχανικά κύματα που μεταδίδονταν σχετικά αργά με ένα μέσο, όπως ένα κύλινδρο γεμάτο με υγρό, υδράργυρο, μαγνητικό πηνίο, ή πιεζοηλεκτρικό κρύσταλλο. Το μέσο μετάδοσης θα μπορούσε να υποστηρίξει τη διάδοση εκατοντάδων ή χιλιάδων παλμών ανά πάσα στιγμή. Μόλις, τα κύματα, έφταναν στο άλλο άκρο του μέσου μετάδοσης, μετατρέπονταν και πάλι σε ηλεκτρικά σήματα, καθυστερημένα κατά το χρόνο μετάδοσής τους στο μέσο. Ο χρόνος αναμονής που απαιτούνταν για να φθάσουν οι παλμοί του ενδιαφέροντός μας στο τέλος του μέσου ήταν συνήθως της τάξης των μικροδευτερολέπτων.

Η βασική ιδέα του συστήματος καθυστέρησης προέρχεται από τις έρευνες κατά την διάρκεια του Β' Παγκόσμιου Πολέμου επάνω στα ραντάρ, ως ένα σύστημα για τη μείωση των ακαταστασίας από αντανακλάσεις από το έδαφος και άλλα "σταθερά" αντικείμενα.

Διάφοροι τύποι συστημάτων καθυστέρησης εφευρέθηκαν για το σκοπό αυτό, με κοινή αρχή ότι οι πληροφορίες αποθηκεύονταν ηχητικά σε ένα μέσο. Το MIT πειραματίστηκε με διάφορα συστήματα, συμπεριλαμβανομένων γυαλί, χαλαζία, χάλυβα και μόλυβδο. Η Ιαπωνία ανέπτυξε ένα σύστημα που αποτελούνταν από ένα στοιχείο

χαλαζία με επίστρωση σκόνης γυαλιού που μείωνε τα επιφανειακά κύματα τα οποία ερχόντουσαν αντίθετα μέσω μιας κατάλληλης υποδοχής. Στις Ηνωμένες Πολιτείες στο Ναυτικό ερευνητικό κέντρο χρησιμοποιούνταν ράβδοι χάλυβα τυλιγμένοι σε μια έλικα, αλλά αυτό ήταν χρήσιμο μόνο για χαμηλές συχνότητες κάτω του 1 MHz.

Το πρώτο πρακτικό de-cluttering σύστημα που βασίζεται στην έννοια αυτή αναπτύχθηκε από τον J. Presper Eckert στο Πανεπιστήμιο της Πενσυλβάνια στην σχολή Moore στο τμήμα Ηλεκτρολόγων Μηχανικών. Η ιδέα του βασιζόταν σε μια στήλη υδραργύρου με πιεζοηλεκτρικούς κρυστάλλους σαν αισθητήρες (συνδυασμός ηχείου και μικροφώνου) στα δύο άκρα.

Μετά τον πόλεμο ο Eckert έστρεψε την προσοχή του στην ανάπτυξη του υπολογιστή. Ένα πρόβλημα με την πρακτική της ανάπτυξης ήταν η έλλειψη κατάλληλης συσκευής μνήμης, και το έργο Eckert σχετικά με τις καθυστερήσεις ραντάρ σήμαινε ότι είχε ένα σημαντικό πλεονέκτημα σε σχέση με άλλους ερευνητές στο θέμα αυτό.

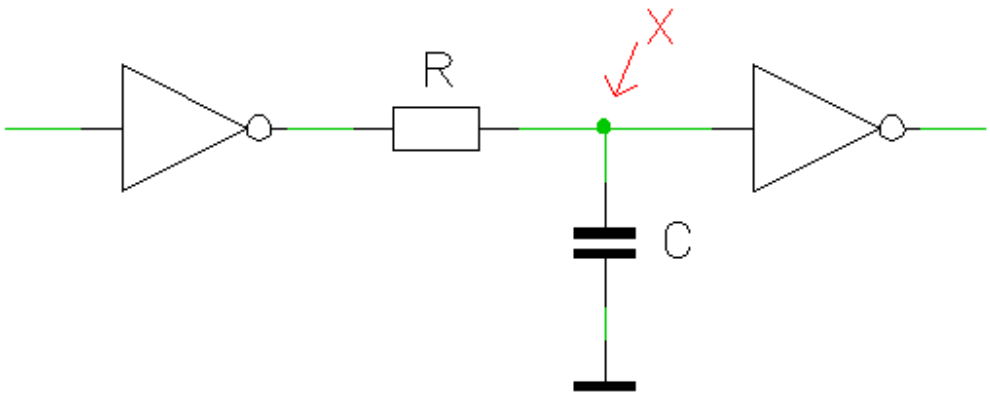
Σήμερα η αλματώδης εξέλιξη των ηλεκτρονικών έχει προσφέρει μια πληθώρα λύσεων για τη δημιουργία καθυστερήσεων χρόνου που σίγουρα καλύπτουν οποιαδήποτε ανάγκη. Τα κυκλώματα αυτά χωρίζονται σε δύο μεγάλες κατηγορίες, αυτά που καθυστερούν αναλογικά ηλεκτρικά σήματα και εκείνα που καθυστερούν παλμούς. Τα γνωστότερα τέτοια κυκλώματα που ανήκουν στην πρώτη κατηγορία είναι αυτά που δημιουργούν ηχώ και βάθος σε σήματα ήχου. Στη δεύτερη κατηγορία ανήκουν κυρίως κυκλώματα που δημιουργούν διαδοχές παλμών για το συγχρονισμό συμβάντων.

Το κύκλωμα που ασχολείται αυτή η εργασία είναι ένα κύκλωμα χρονικής καθυστέρησης παλμών.

ΚΕΦΑΛΑΙΟ 3

ΤΡΟΠΟΙ ΠΟΥ ΧΡΗΣΙΜΟΠΟΙΟΥΝΤΑΙ ΓΙΑ ΝΑ ΕΠΙΤΕΥΧΘΕΙ ΧΡΟΝΙΚΗ ΚΑΘΥΣΤΕΡΗΣΗ ΣΤΑ ΗΛΕΚΤΡΟΝΙΚΑ

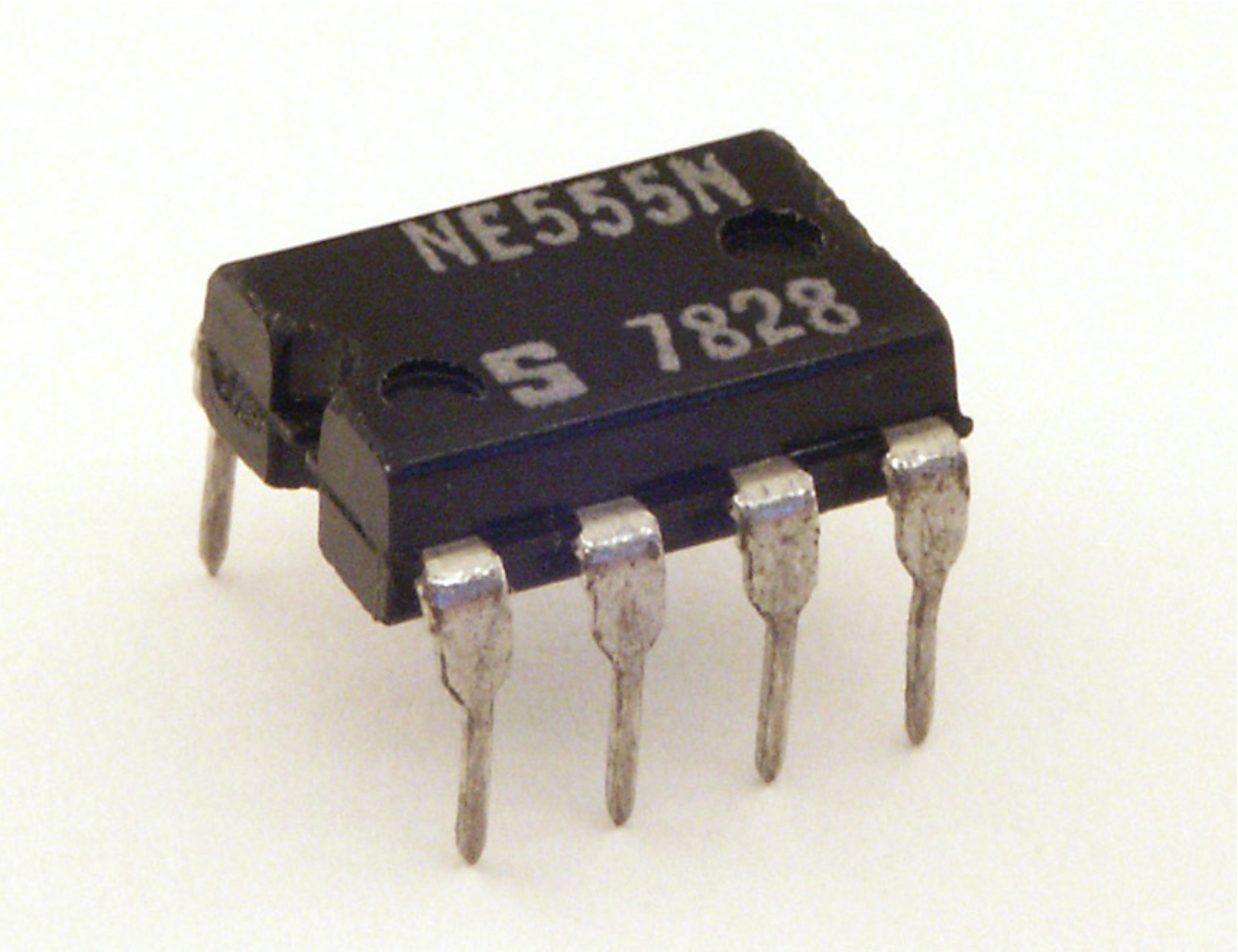
3.1 RC ΜΟΝΑΔΑ ΚΑΘΥΣΤΕΡΗΣΗΣ



Σχ. 1. Κύκλωμα RC

Η πιο συνηθισμένη μέθοδος για τη παραγωγή χρονοκαθυστερήσεων παλμών στα ηλεκτρονικά χρησιμοποιεί ένα δικτύωμα αντίστασης – πυκνωτή (RC)[1], όπως φαίνεται στο Σχ.1. Σήμερα είναι διαθέσιμη μια ποικιλία ολοκληρωμένων κυκλωμάτων που μπορούν να παραγάγουν καθυστέρηση χρόνου χρησιμοποιώντας ένα δικτύωμα RC . Το πιο δημοφιλές από αυτά είναι το 555 σε συνδεσμολογία μονοσταθούς πολυδονητή.

3.2 RC ΜΟΝΟΣΤΑΘΗΣ ΠΟΛΥΔΟΝΗΤΗΣ 555



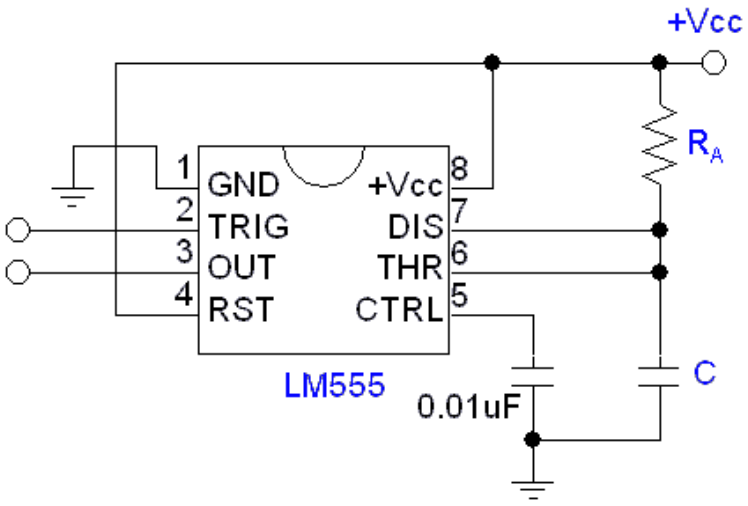
Σχ. 2. RC 555 μονοσταθής πολυδονητής

Σε λειτουργία μονοσταθή πολυδονητή[3], ο χρονιστής 555 λειτουργεί ως κύκλωμα «μίας βολής» (one-shot). Η συνδεσμολογία για να επιτευχθεί ένα τέτοιο κύκλωμα φαίνεται στο Σχ. 3. Αρχικά ο πυκνωτής είναι πλήρως εκφορτισμένος και διατηρείται έτσι από τον ακροδέκτη “discharge”. Όταν στο κύκλωμα έλθει ένας παλμός ενεργοποίησης (αρνητικό μέτωπο στον ακροδέκτη “trigger” ο πυκνωτής C αρχίζει να φορτίζει μέσω της αντίστασης R_A. Όταν η τάση στα άκρα του πυκνωτή φτάσει στα 2/3 της τάσης τροφοδοσίας τότε θα εμφανιστεί στην έξοδο του κυκλώματος ένα αρνητικό μέτωπο. Η χρονική καθυστέρηση εξαρτάται από τη σταθερά χρόνου «τ» (τ= RC).

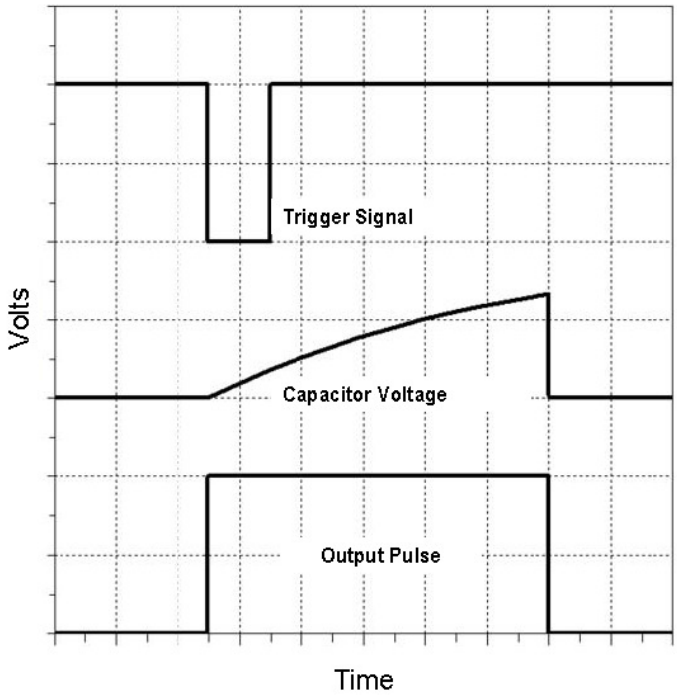
Η χρονική καθυστέρηση t είναι ουσιαστικά ο χρόνος που χρειάζεται για να ανέβει η τάση στον πυκνωτή C στα 2/3 της τάσης τροφοδοσίας και δίνεται από τον τύπο:

$$t = 1,1\ RC$$

όπου t σε δευτερόλεπτα, R είναι σε Ohm και C είναι σε farads.



Σχ. 3. Κύκλωμα RC 555 μονοσταθή πολυδονητή



Σχ. 4. Οι σχέσεις του σήματος ενεργοποίησης, η τάση για την Γ και του εύρους του παλμού στο μονοσταθής λειτουργία

Τα κυκλώματα καθυστέρησης χρόνου RC αποτελούν μια απλή και αξιόπιστη λύση. Όμως στην επίτευξη πολύ μεγάλων και πολύ μικρών χρόνων καθυστέρησης παρουσιάζουν προβλήματα. Στους πολύ μεγάλους χρόνους (>1hr) το ρεύμα φόρτισης της χωρητικότητας μικραίνει πολύ με αποτέλεσμα η διαρροή της χωρητικότητας και η αντίσταση εισόδου του παράλληλου κυκλώματος να δημιουργούν σημαντικά σφάλματα στον χρόνο καθυστέρησης. Σε πολύ μικρούς χρόνους (της τάξης των nsec) ο έλεγχος του χρόνου καθυστέρησης, ο οποίος γίνεται συνήθως με κάποια μεταβλητή αντίσταση, εισάγει προβλήματα και καθώς η χωρητικότητα και η αντίσταση αποκτούν πολύ χαμηλές τιμές το κόστος του υπόλοιπου κυκλώματος ανεβαίνει προκειμένου να διατηρηθεί η αξιοπιστία του. Έτσι για τους ζητούμενους χρόνους αυτής της εργασίας (της τάξεως του ns) η μέθοδος αυτή δεν κρίνεται κατάλληλη.

3.3 ΧΡΟΝΙΣΤΕΣ (TIMERS) ΣΤΟΥΣ ΜΙΚΡΟΕΛΕΓΚΤΕΣ

Μια ειδική κατηγορία ενσωματωμένων περιφερειακών συσκευών στους μικροελεγκτές είναι οι χρονιστές. Στην ουσία πρόκειται για ενσωματωμένους μετρητές στον μικροελεγκτή που αυξάνουν ή μειώνουν την τιμή του περιεχομένου τους κατά μια μονάδα με κάθε παλμό χρονισμού. Η μεταβολή αυτή γίνεται σε περιοδικά χρονικά διαστήματα που ορίζει ο προγραμματιστής.

Στη λειτουργία του χρονιστή [4], ο προγραμματιστής ορίζει το χρονικό διάστημα κάθε παλμού τον οποίο μετρά ο μετρητής και όταν αυτό περατωθεί, ο χρονιστής αυξάνει (ή μειώνει) το περιεχόμενό του κατά 1. Ο μετρητής συνήθως προφορτώνεται με μια συγκεκριμένη τιμή και όταν αυτός γεμίσει πχ. με την τιμή 0xFF τότε κατά την μετάβασή του στην επόμενη κατάσταση συμβαίνει υπερχείλιση (overflow) και μεταπίπτει στην τιμή η 0x00. Το συμβάν αυτό μπορεί να προκαλέσει ένα αίτημα διακοπής (iinterrupt) ή να αλλάξει την λογική κατάσταση σε ένα ακροδέκτη του μικροελεγκτή.

μικροεπεξεργαστή του συστήματος.

Με χρήση των χρονιστών ο προγραμματιστής, μπορεί να προγραμματίσει λειτουργίες του μικροελεγκτή να γίνονται σε συγκεκριμένα χρονικά διαστήματα που απαιτεί η εφαρμογή που θέλει να αναπτύξει. Το χρονικό διάστημα ορίζεται μέσω επιλεγόμενων υποδιαιρέσεων του κυκλώματος χρονισμού του μικροελεγκτή. Ουσιαστικά μετρά παλμούς ρολογιού. Ο προγραμματιστής ορίζει κάθε πόσους παλμούς ρολογιού θα αυξάνει ο απαριθμητής την τιμή του κατά 1.

Τα κυκλώματα καθυστέρησης χρόνου που είναι στηριγμένα σε μικροελεγκτές είναι συνήθως φιλικά στον χρήστη και μπορούν με άνεση και με ακρίβεια να μετρήσουν πολύ μεγάλα διαστήματα καθυστέρησης. Στα μικρά διαστήματα καθυστέρησης παρουσιάζουν πρόβλημα γιατί υπάρχει άμεση εξάρτηση με τον χρόνο περιόδου του

παλμού χρονισμού του μικροελεγκτή που περιέχει τους χρονιστές, με αποτέλεσμα να χρειάζονται εξαιρετικά γρήγορα τέτοια ολοκληρωμένα κυκλώματα. Ένα άλλο πρόβλημα είναι ο συγχρονισμός του σήματος εισόδου με τον παλμό χρονισμού (που είναι αναπόφευκτος στα σύγχρονα ψηφιακά κυκλώματα) με αποτέλεσμα την ύπαρξη χρόνου αβεβαιότητας (jitter) που μειώνει την ακρίβεια στα κυκλώματα αυτά.

Ένα ακόμα μειονέκτημα των μικροελεγκτών, που στις συνηθισμένες τους χρήσεις δεν είναι εμφανές, είναι η ευαισθησία τους σε υψηλές τιμές ηλεκτρομαγνητικού θορύβου. Φυσικά το πρόβλημα είναι γνωστό στους κατασκευαστές που τους εφοδιάζουν πλέον με ειδικά κυκλώματα που ελέγχουν τη λειτουργία τους (π.χ. watchdog timer) και τους επαναφέρουν στην πρέπουσα κατάσταση αν παρουσιαστούν τέτοια προβλήματα. Ακόμα και έτσι όμως η χρήση μικροελεγκτών σε εργαστήρια που παράγονται ηλεκτρομαγνητικοί παλμοί είναι προβληματική.

Για τα προβλήματα που παρουσιάζουν τα κυκλώματα χρονισμού που χρησιμοποιούν μικροελεγκτές, τα οποία είναι σημαντικά για την εφαρμογή αυτής της εργασίας, η μέθοδος αυτή κρίθηκε ακατάλληλη για την υλοποίηση του κυκλώματός μας.

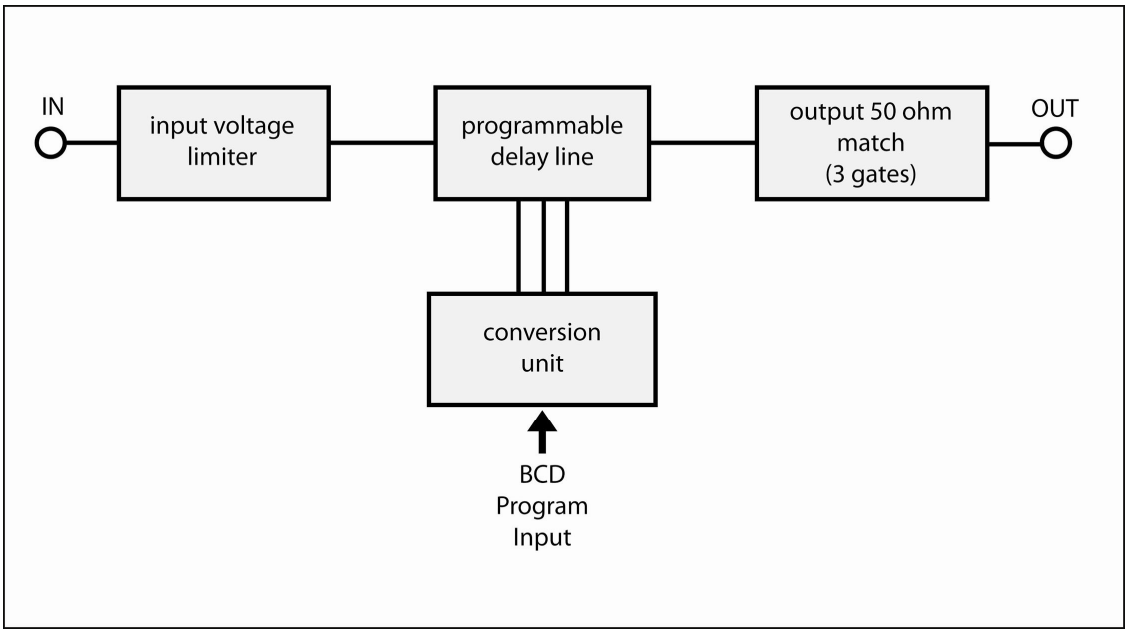
ΚΕΦΑΛΑΙΟ 4
ΜΟΝΑΔΑ ΚΑΘΥΣΤΕΡΗΣΗΣ (TTL)

4.1 ΜΟΝΑΔΑ ΚΑΘΥΣΤΕΡΗΣΗΣ με χρήση ολοκληρωμένων κυκλωμάτων γραμμής καθυστέρησης (Delay-Line):

Το πρόβλημα της σύντομης καθυστέρησης παλμών έχει απασχολήσει τις εταιρείες κατασκευής ολοκληρωμένων κυκλωμάτων που σήμερα διαθέτουν μια ποικιλία προγραμματιζόμενων ολοκληρωμένων κυκλωμάτων που υλοποιούν γραμμές καθυστέρησης. Η γραμμή καθυστέρησης υλοποιείται σε αυτά τα ολοκληρωμένα από μια σειρά από λογικές πύλες που κατασκευάζονται να έχουν αυστηρά καθορισμένη καθυστέρηση διάδοσης. Μέσω του προγραμματισμού ο χρήστης μπορεί να επιλέξει τον αριθμό των πυλών που θα έχει τοποθετημένες σε σειρά και με αυτό τον τρόπο καθορίζει και την επιθυμητή καθυστέρηση. Τα ολοκληρωμένα αυτά αποτελούν μια πολύ καλή και αξιόπιστη λύση στο πρόβλημα της χρονικής καθυστέρησης παλμών και για αυτό και επιλέχθηκαν για την υλοποίηση της συγκεκριμένης εργασίας.

Η φιλοσοφία της μονάδας καθυστέρησης που κατασκευάσαμε παρουσιάζεται στο παρακάτω block διάγραμμα :

4.2 BLOCK ΔΙΑΓΡΑΜΜΑ:

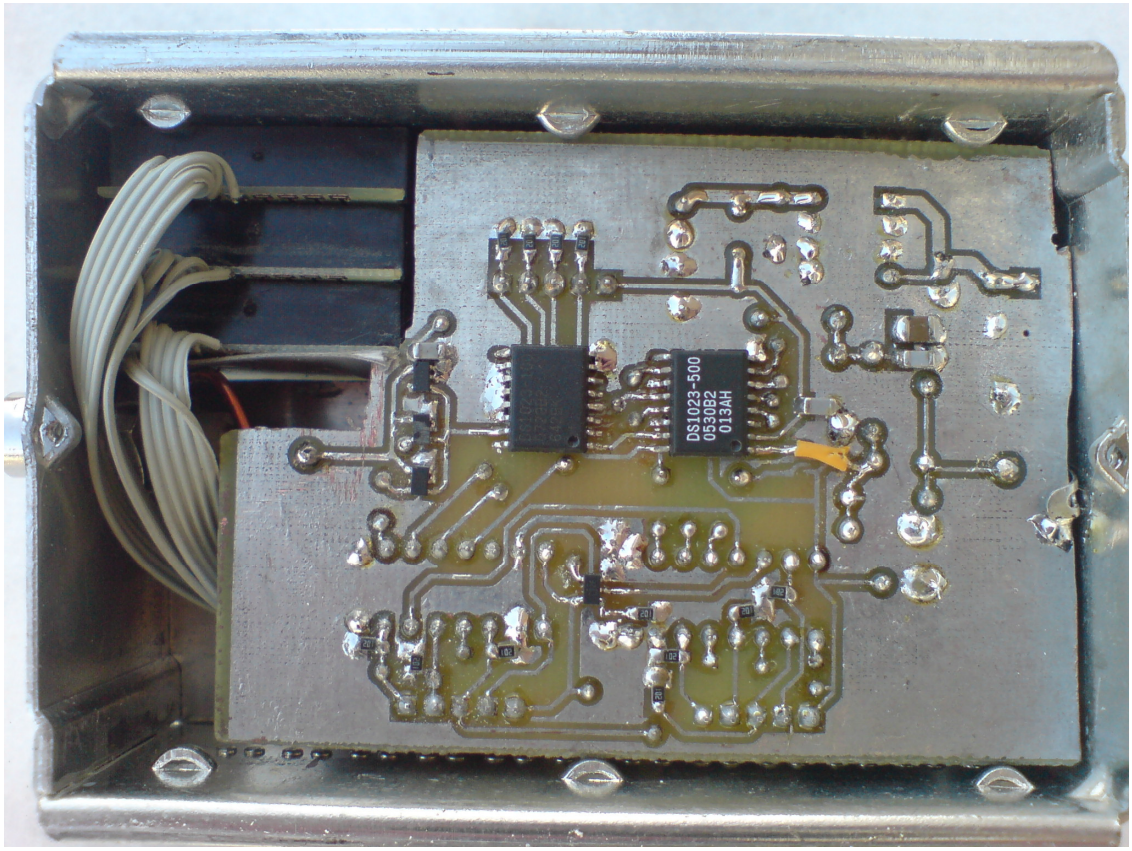


Το σήμα εισόδου οδηγείται αρχικά σε ένα κύκλωμα ψαλιδιστή με διόδους. Ο ψαλιδιστής αυτός (input voltage limiter) περιορίζει την τάση εισόδου στο υπόλοιπο κύκλωμα έτσι ώστε αυτή να είναι πάντα μέσα στην περιοχή 0V με 5V. Με τον τρόπο αυτό το υπόλοιπο κύκλωμα προστατεύεται από υπερτάσεις που μπορεί να δημιουργηθούν στην είσοδο από ηλεκτρομαγνητικό θόρυβο.

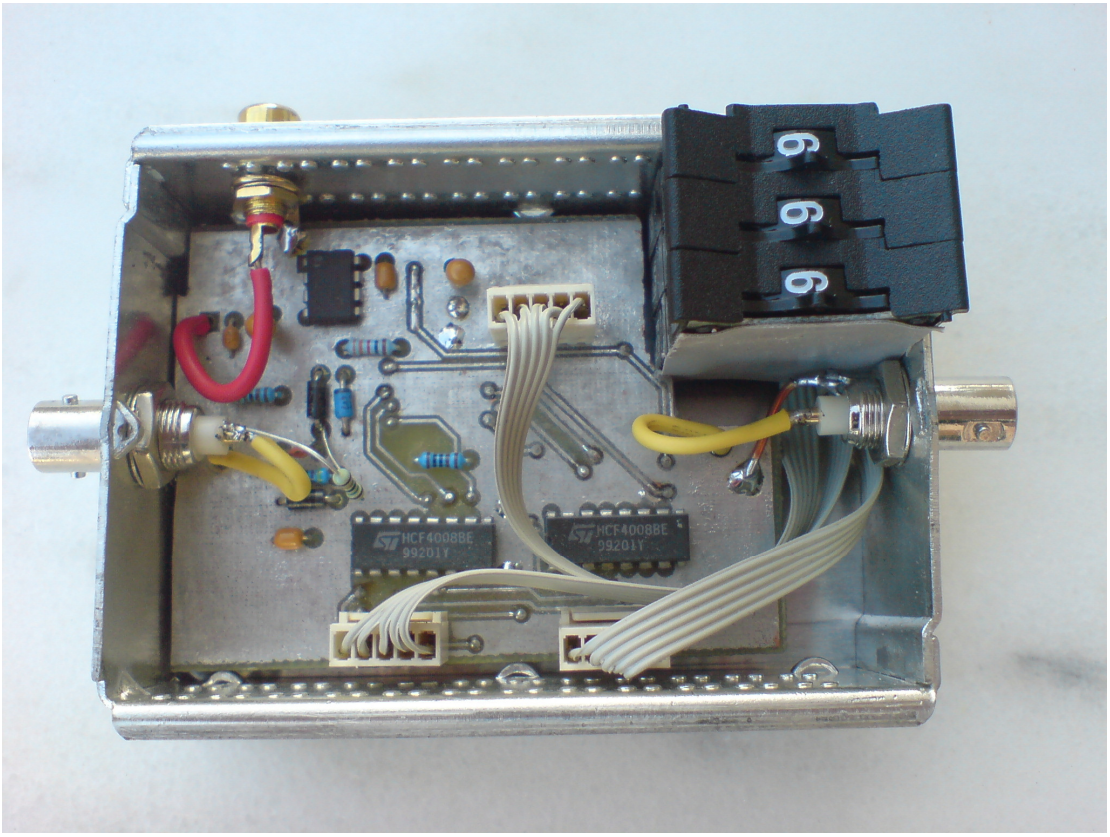
Στην συνέχεια έχουμε το κύκλωμα καθυστέρησης (programmable delay line) το οποίο αποτελείται από δύο ολοκληρωμένα κυκλώματα γραμμών καθυστέρησης (delay lines). Το ένα ολοκληρωμένο έχει βήμα καθυστέρησης 1ns και έχει συνδεσμολογηθεί Ο προγραμματισμός του γίνεται απευθείας από ένα δεκαδικό περιστροφικό διακόπτη (thumb wheel) και έτσι μετράει το πολύ 10 βήματα (0-9 ns).Το δεύτερο ολοκληρωμένο έχει βήμα καθυστέρησης

5ns και έχει συνδεσμολογηθεί με τέτοιο τρόπο ώστε να μετρά ανά δύο βήματα για να δώσει τελικά βήμα 10ns και συνδέεται σε σειρά με το πρώτο με σκοπό να δημιουργήσει τις δεκάδες των καθυστερήσεων. Το ολοκληρωμένο παρέχει 256 βήματα καθυστέρησης από τα οποία χάνονται τα μισά επειδή μετρά ανά δύο βήματα και έτσι έχουμε διαθέσιμα 128 βήματα. Ο προγραμματισμός του μπορεί να επιτευχθεί με δύο δεκαδικούς περιστροφικούς διακόπτες, με μόνο πρόβλημα ότι η είσοδος προγραμματισμού του ολοκληρωμένου είναι δυαδική ενώ η έξοδος των διακοπτών είναι τελικά BCD (Binary Coded Decimal). Έτσι χρησιμοποιούνται δύο δεκαδικοί περιστροφικοί διακόπτες που συνδέονται σε έναν μετατροπέα BCD σε BINARY έτσι ώστε το δεύτερο ολοκληρωμένο να μετράει 100 βήματα (0-990ns). Με αυτό το τρόπο το σήμα περνά από τα δύο ολοκληρωμένα κυκλώματα γραμμών καθυστέρησης και παίρνει την επιθυμητή καθυστέρηση. Πριν όμως οδηγηθεί στην έξοδο (OUT) οδηγείται σε τρεις λογικές πύλες υψηλής ταχύτητας και δυνατότητας παροχής μεγάλου ρεύματος, οι οποίες λειτουργούν παράλληλα και παρέχουν τα απαιτούμενα 100 mA στα 5 V για να έχει το κύκλωμα τη δυνατότητα οδήγησης φορτίων με χαρακτηριστική αντίσταση τόσο χαμηλή όσο τα 50 Ω.

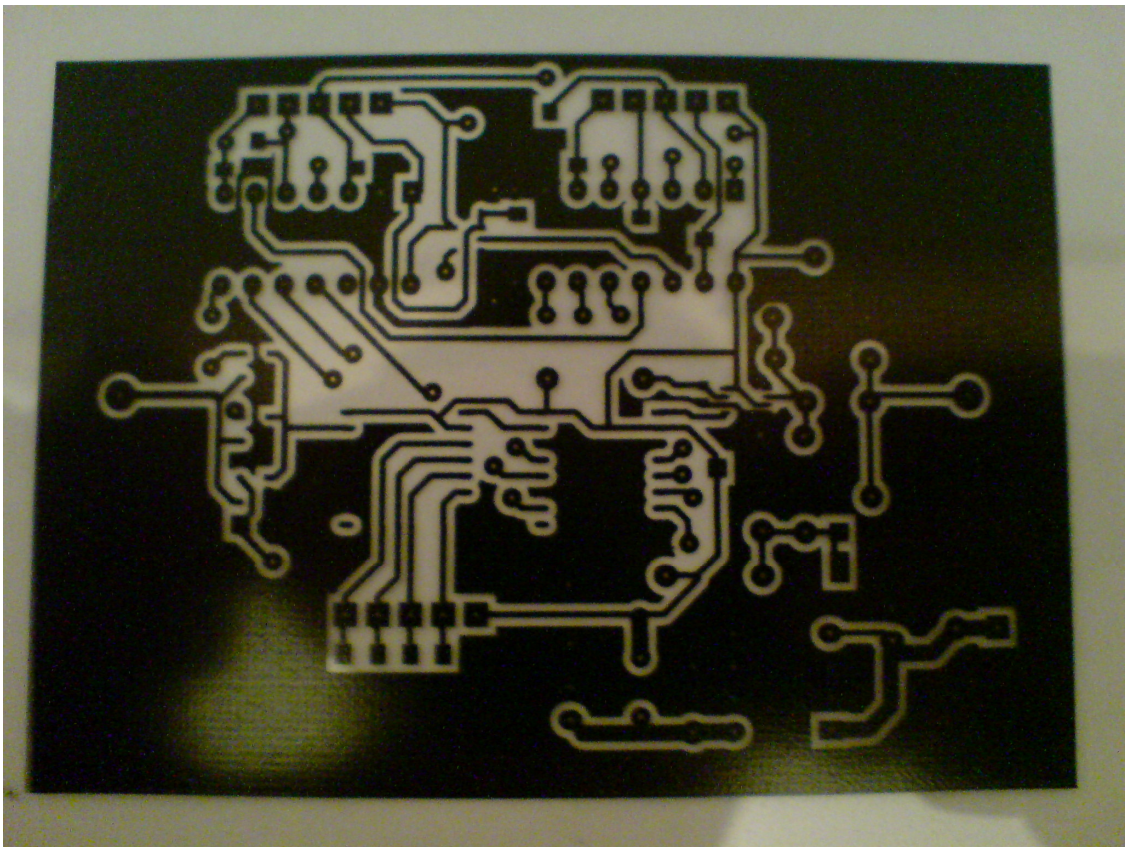
4.3 ΦΩΤΟΓΡΑΦΙΚΟ ΥΛΙΚΟ:



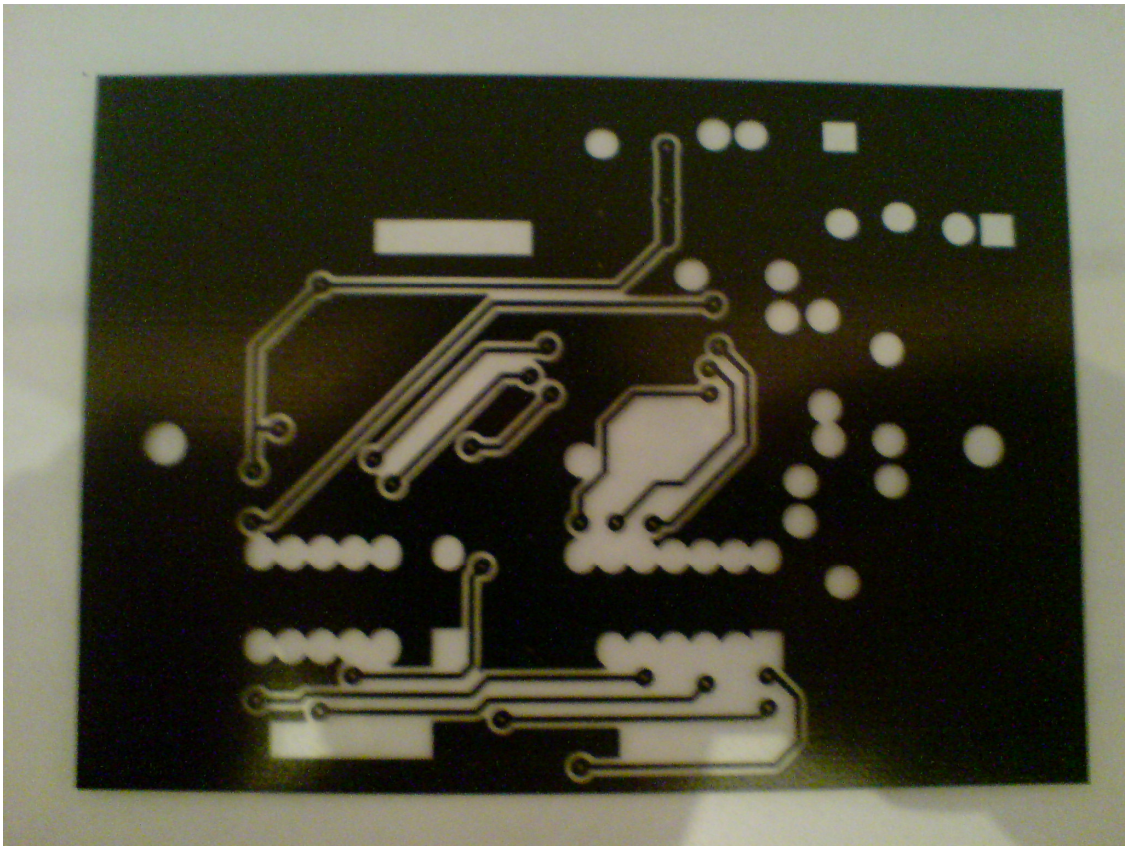
Μονάδα καθυστέρησης όψη 1



Μονάδα καθυστέρησης όψη 2



Διαφάνεια κυκλώματος όψη 1



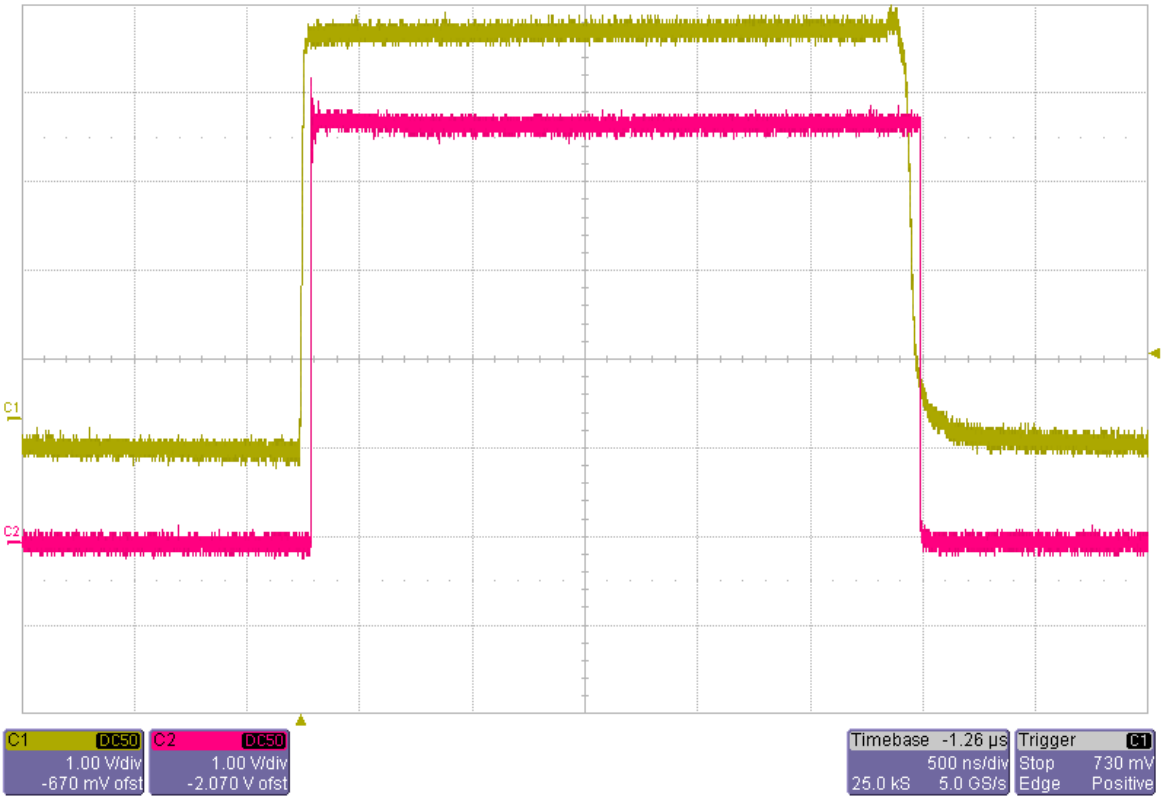
Διαφάνεια κυκλώματος όψη 2

ΚΕΦΑΛΑΙΟ 5

ΕΡΓΑΣΤΗΡΙΑΚΕΣ ΜΕΤΡΗΣΕΙΣ

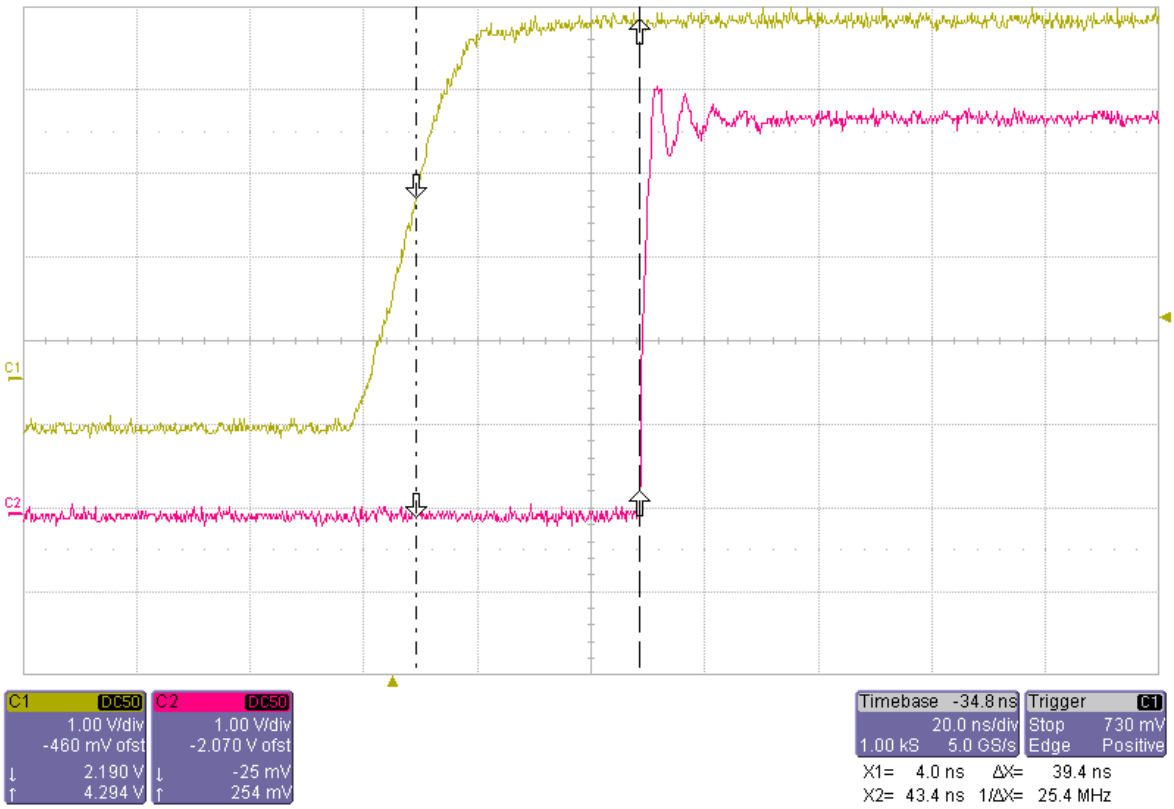
Παρακάτω φαίνονται οι κυματομορφές των τάσεων εισόδου και εξόδου για διάφορες καθυστερήσεις. Επίσης πραγματοποιείται σύγκριση της μονάδος καθυστέρησης που κατασκευάστηκε με αντίστοιχη μονάδα καθυστέρησης που υπάρχει στο εργαστήριο.

5.1 ΤΑΣΕΙΣ ΕΙΣΟΔΟΥ - ΕΞΟΔΟΥ



Οι τάσεις εισόδου (C1) – εξόδου (C2) χωρίς καθυστέρηση (ελάχιστη καθυστέρηση).

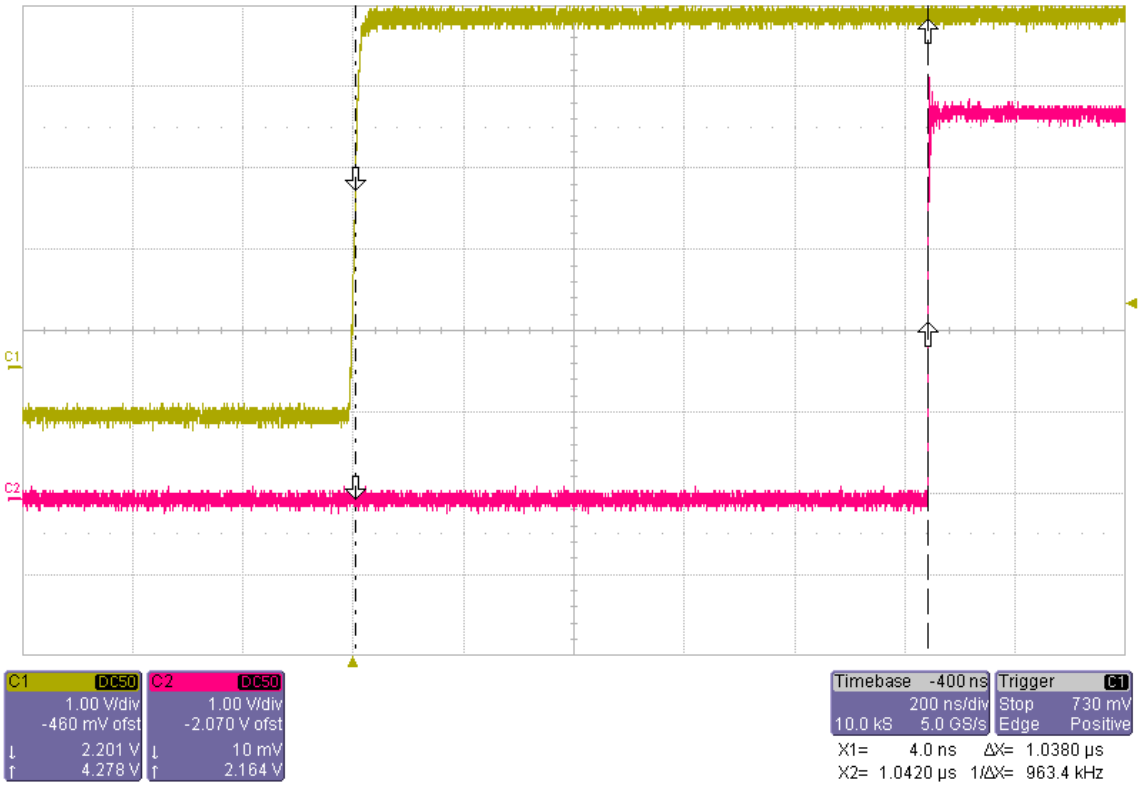
5.2 ΜΕΤΡΗΣΗ ΕΛΑΧΙΣΤΟΥ ΧΡΟΝΟΥ



Τάσεις εισόδου (C1) – εξόδου (C2). Μέτρηση ελάχιστης καθυστέρησης (κυκλώματος)

-Εδώ παρατηρούμε ότι έχοντας ορίσει την καθυστέρηση μας στα 0 ns υπάρχει μία μικρή καθυστέρηση (39,4) ns η οποία ονομάζεται ελάχιστη καθυστέρηση και οφείλεται στο κύκλωμα της μονάδας μας.

5.3 ΜΕΤΡΗΣΗ ΜΕΓΙΣΤΟΥ ΧΡΟΝΟΥ

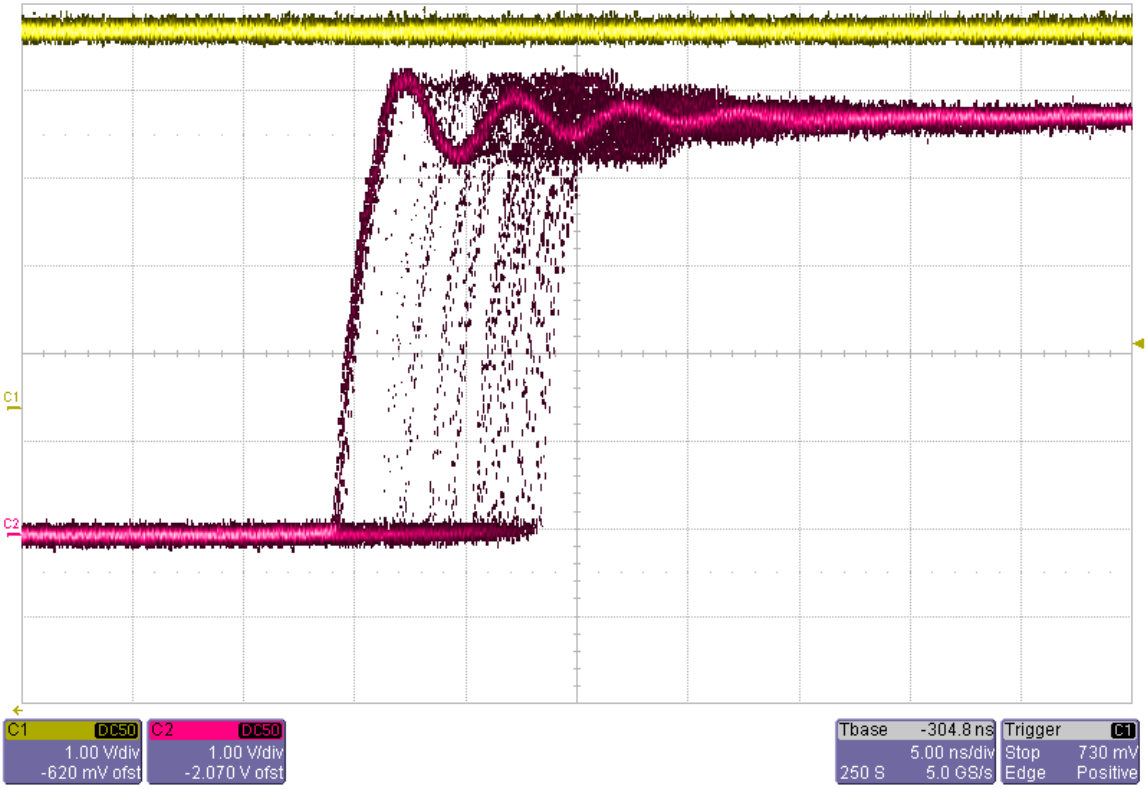


Τάσεις εισόδου (C1) – εξόδου (C2).Μέγιστη καθυστέρηση

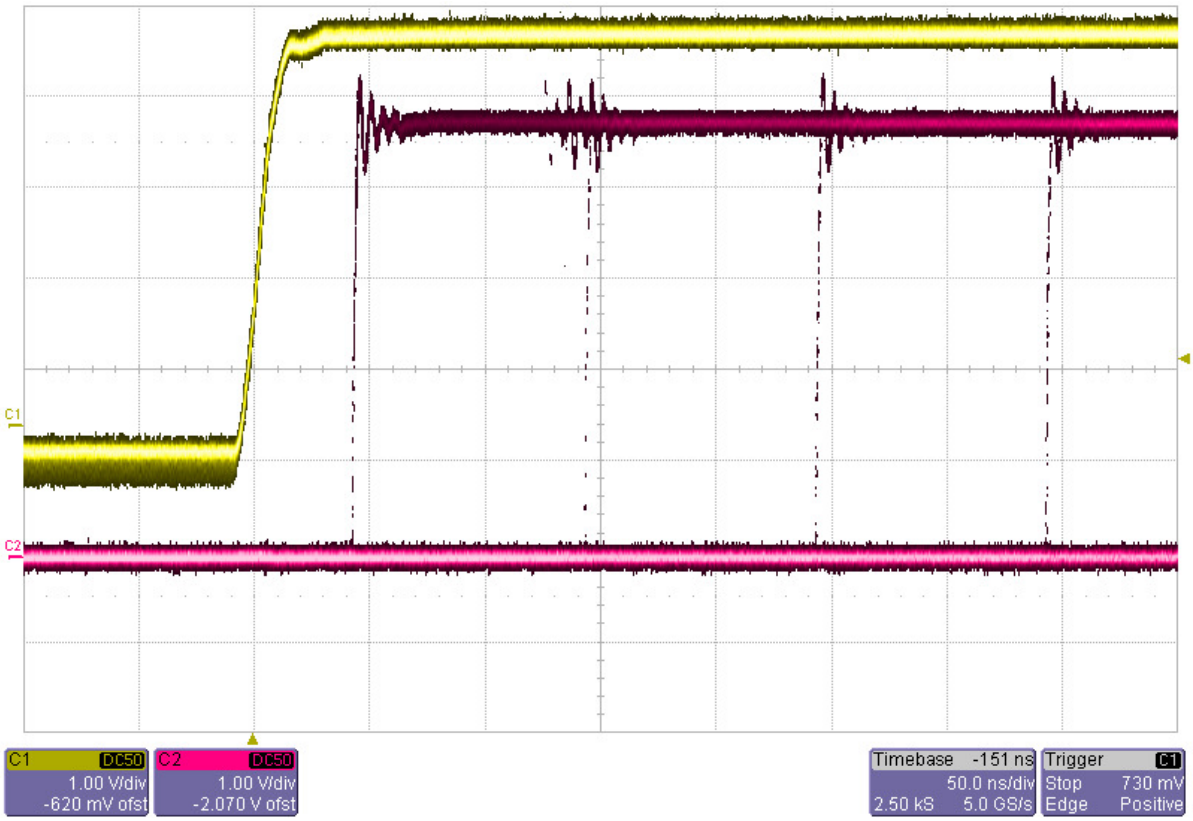
-Στη συνέχεια βλέπουμε την μέγιστη καθυστέρηση που μπορεί να πετύχει η μονάδα μας.Η οποία είναι 1038 ns.Είναι αναμενόμενο αυτό το αποτέλεσμα καθώς η μονάδα είναι κατασκευασμένη για να καλύπτει καθυστερήσης εύρους 0-1000 ns.Επομένως αν υπολογίσουμε και την ελάχιστη καθυστέρηση λόγω κυκλώματος που είχαμε παραπάνω η οποία ήταν 39,4 ns τελικά προκύπτει ότι θα έχουμε συνολική καθυστέρηση περίπου 1038 ns.

5.4 ΤΑΣΕΙΣ ΤΥΧΑΙΩΝ ΚΑΘΥΣΤΕΡΗΣΕΩΝ

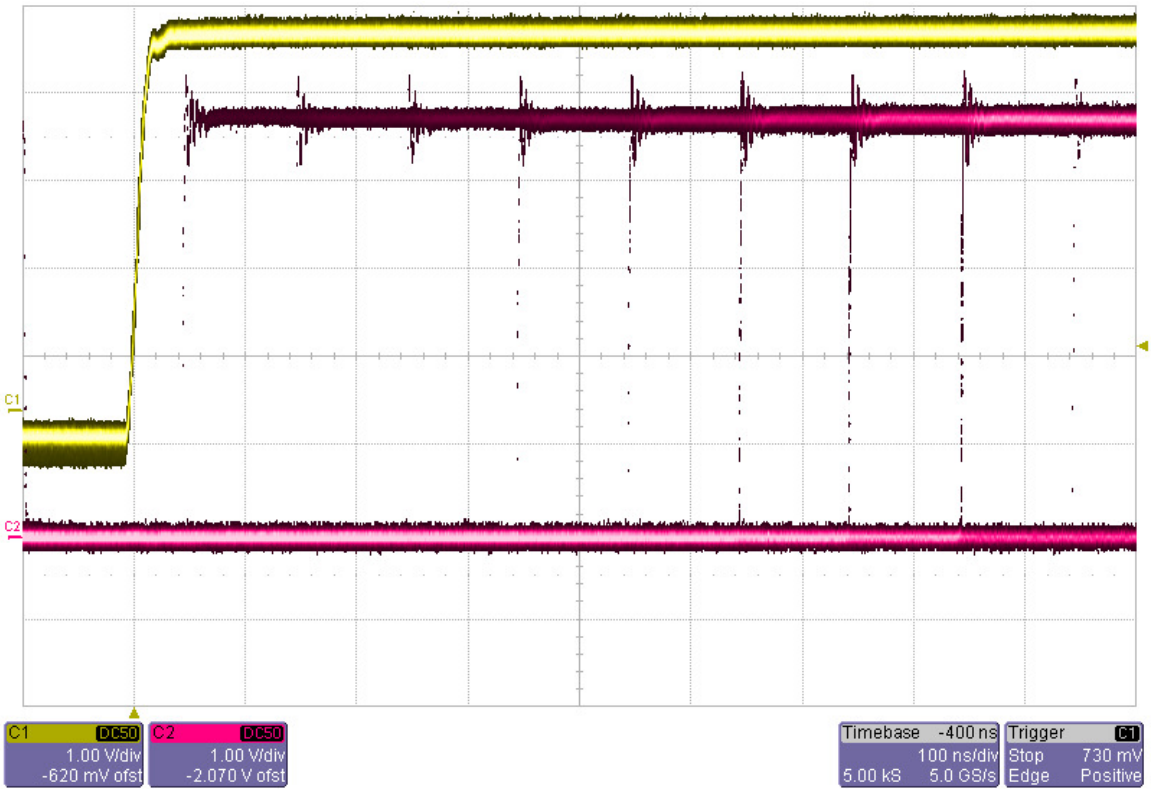
Παρακάτω θα δείξουμε μερικές κυματομορφές τάσεων για διαφορετικές τιμές καθυστερήσεων



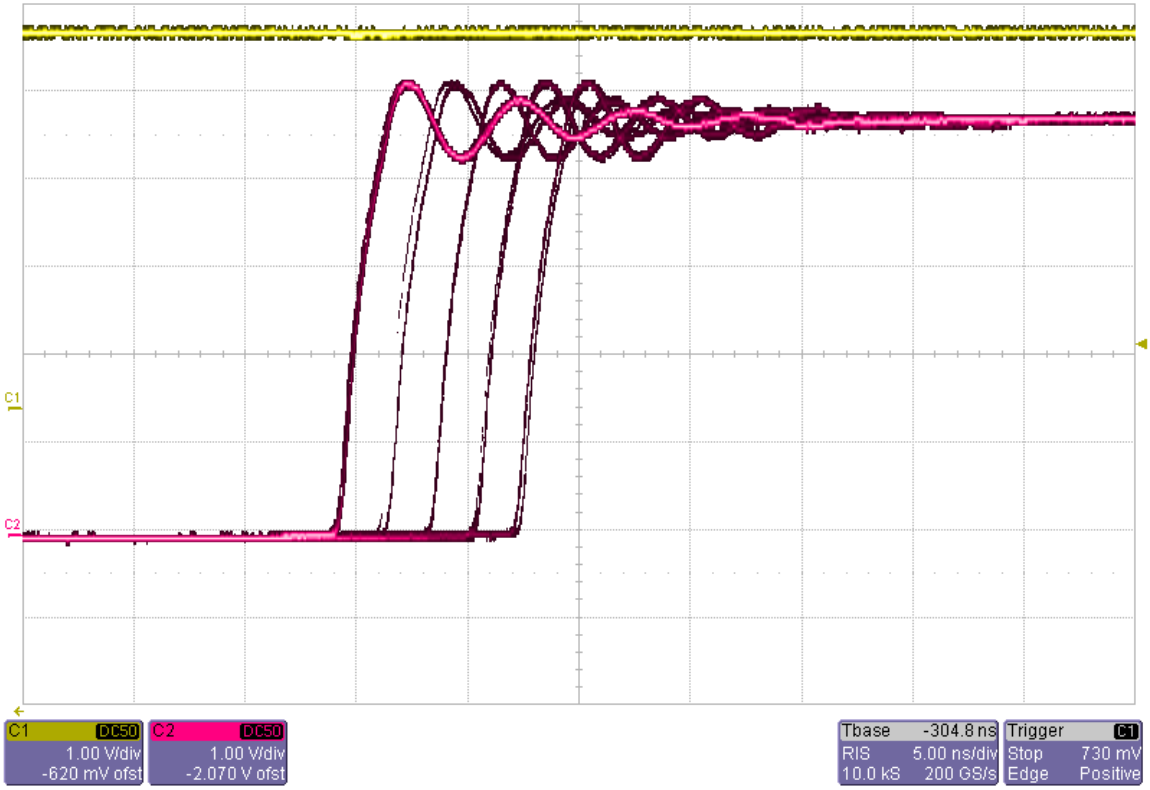
Διαδοχικές καθυστερήσεις τάσεως στην έξοδο ανά 1 ns (κλίμακα 5 ns/υποδιαίρεση)



Διαδοχικές καθυστερήσεις τάσεως στην έξοδο ανά 100 ns (κλίμακα 50 ns/ υποδιαίρεση)

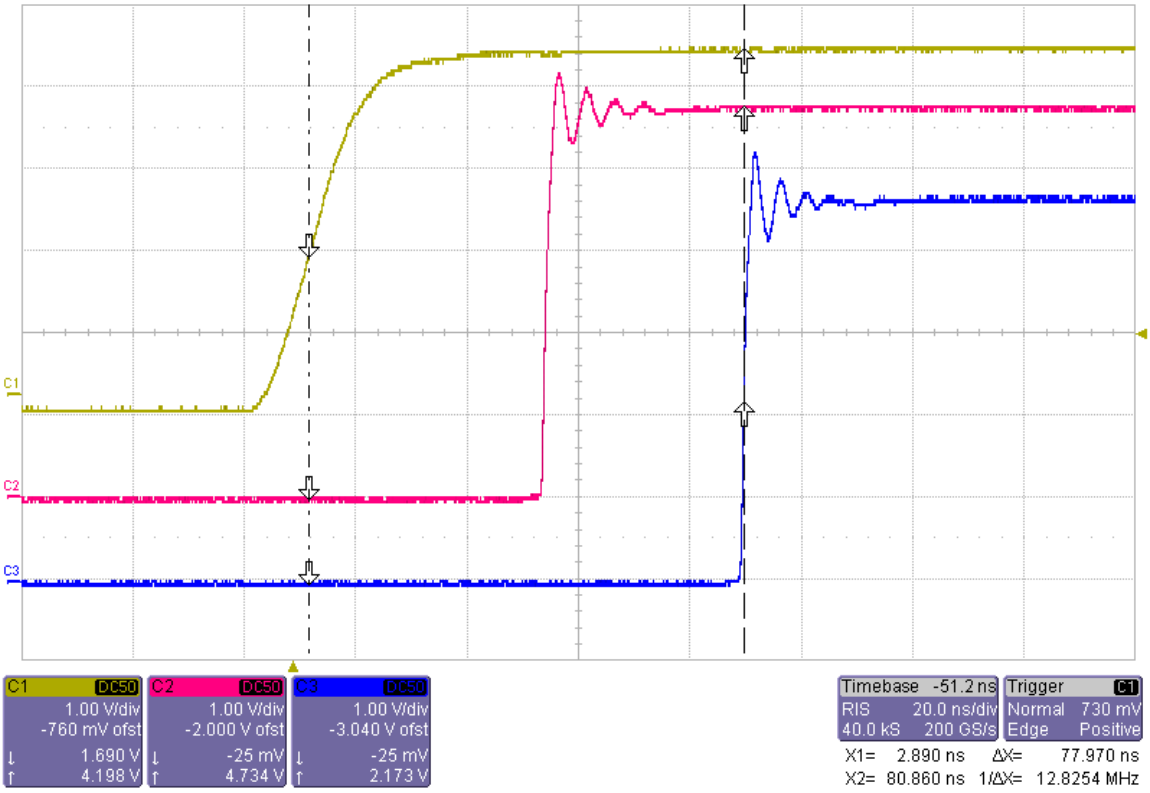


Διαδοχικές καθυστερήσεις τάσεως στην έξοδο ανά 100 ns (κλίμακα 100 ns/ υποδιαίρεση)



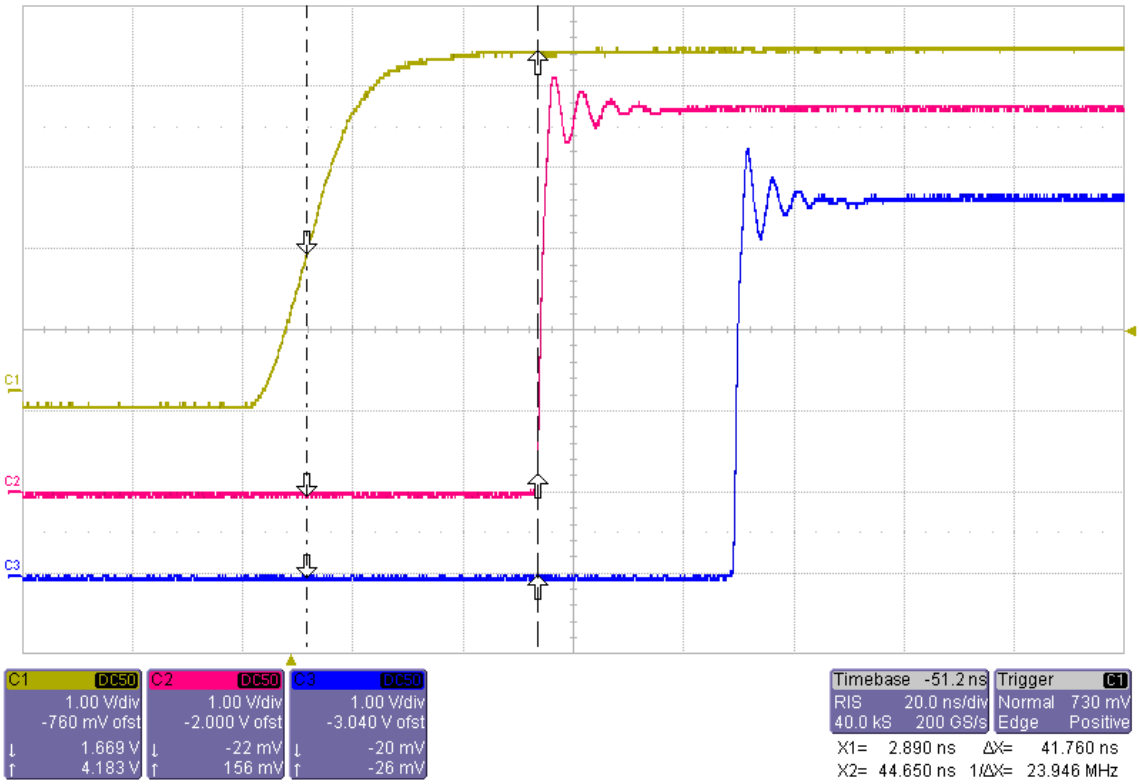
Τυχαίες διαδοχικές καθυστερήσεις τάσεως στην έξοδο (κλίμακα 5 ns/ υποδιαίρεση)

5.5 ΣΥΓΚΡΙΣΗ ΜΟΝΑΔΑΣ ΚΑΘΥΣΤΕΡΗΣΗΣ ΠΟΥ ΚΑΤΑΣΚΕΥΑΣΤΗΚΕ ΜΕ ΜΟΝΑΔΑ ΚΑΘΥΣΤΕΡΗΣΗΣ ΠΟΥ ΠΡΟΫΠΗΡΧΕ ΣΤΟ ΕΡΓΑΣΤΗΡΙΟ



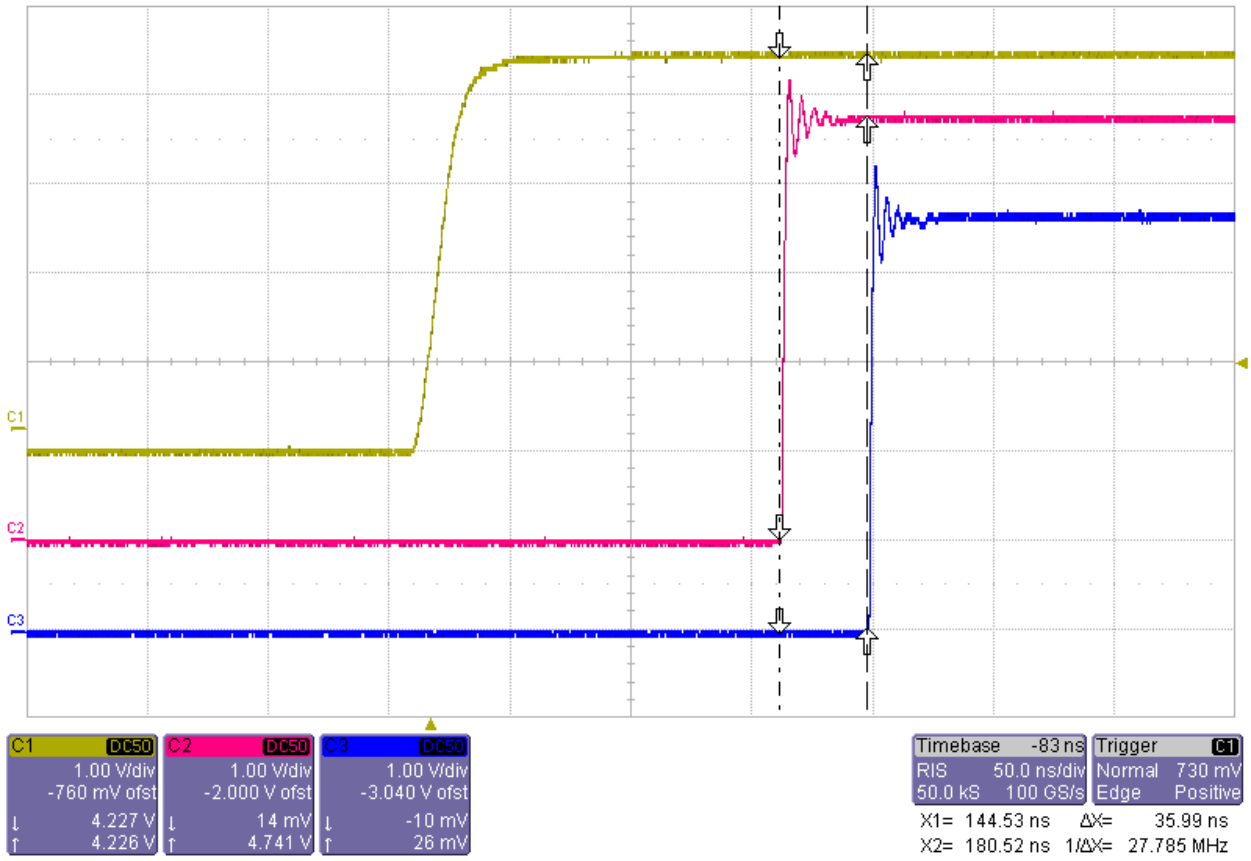
Σύγκριση μονάδων καθυστέρησης-Ελάχιστη καθυστέρηση μονάδας εργαστηρίου

-Εδώ βλέπουμε την ελάχιστη καθυστέρηση (καθυστέρηση κυκλώματος) της μονάδας που είχε κατασκευαστεί παλαιότερα στο εργαστήριο και συγκρίνεται με την μονάδα που κατασκευάστηκε τώρα. Η συνολική ελάχιστη καθυστέρηση της μονάδας αυτής είναι περίπου 78 ns



Σύγκριση μονάδων καθυστέρησης-Ελάχιστη καθυστέρηση μονάδας που κατασκευάστηκε

-Εδώ έχουμε την ελάχιστη καθυστέρηση (καθυστέρηση κυκλώματος) της μονάδας που κατασκευάστηκε τώρα στο εργαστήριο. Η συνολική ελάχιστη καθυστέρηση της μονάδας αυτής είναι περίπου 41 ns.. Σε προηγούμενη μέτρηση είχαμε βρει ότι ήταν 39,4 ns.Οι δυο μετρήσεις είναι πολύ κοντά και τα σφάλματα του παλμογράφου δικαιολογούν αυτή την απόκλιση.



Σύγκριση μονάδων καθυστέρησης-Διαφορά ελάχιστων καθυστερήσεων

-Εδώ παρατηρούμε ότι υπάρχει διαφορετική ελάχιστη καθυστέρηση ανάμεσα στις δύο μονάδες. Το παραπάνω διάγραμμα τάσεων μας δείχνει ότι η διαφορά των ελάχιστων καθυστερήσεων των δύο μονάδων είναι περίπου 36 ns

5.6 ΣΥΜΠΕΡΑΣΜΑΤΑ

Με βάση τα αποτελέσματα των μετρήσεων που πραγματοποιήσαμε παρατηρούμε ότι το σύστημά μας είναι ακριβές ενώ ταυτόχρονα το περιβάλλον για το χρήστη είναι πιο φιλικό δίνοντάς του παράλληλα μεγάλες δυνατότητες για καθυστερήσεις της τάξεως του νανοδευτερολέπτου.

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1. Ηλεκτρονική MALVINO 6η έκδοση

2. Ηλεκτρονικά Ισχύος MOHAN - UNDELAND - ROBBINS
   Β' έκδοση

3.van Roon, Tony (1995). "555 Timer Tutorial" Tony van Roon (VA3AVR) Website. Retrieved 2010-04-05.

4. Ειδικά κεφάλαια μικροθεωρία - Δρ. Σ.Ν. Μπουλταδάκης

5. INTERNET

ΠΑΡΑΡΤΗΜΑ: DATA SHEET ΣΤΟΙΧΕΙΩΝ ΚΥΚΛΩΜΑΤΟΣ

CD4008BMS

CMOS 4-Bit Full Adder With Parallel Carry Out

November 1994

Features

- **High-Voltage Type (20V Rating)**
- **4 Sum Outputs Plus Parallel Look-ahead Carry-Output**
- **High-Speed Operation - Sum In-To-Sum Out, 160ns Typ; Carry In-To-Carry Out, 5ns Typ. At VDD = 10V, CL=50pF**
- **Standardized Symmetrical Output Characteristics**
- **100% Tested For Quiescent Current At 20V**
- **Maximum Input Current of 1μa at 18V Over Full Package-Temperature Range;**
  - **100nA at 18V and 25°C**
- **Noise Margin (Over Full Package Temperature Range):**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **5V, 10V and 15V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

- **Binary Addition/Arithmetic Units**

Description

CD4008BMS types consist of four full adder stages with fast look ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" but to permit high-speed operation in arithmetic sections using several CD4008BMS's.

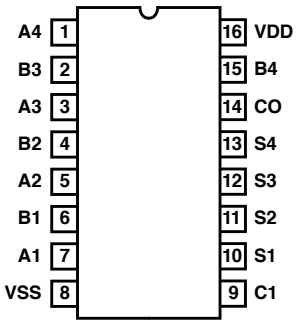
CD4008BMS inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the "Carry In" bit from a previous section. CD4008BMS outputs include the four sum bits, S1 to S4. In addition to the high speed "parallel-carry-out" which may be utilized at a succeeding CD4008BMS section.

The CD4008BMS is supplied in these 16-lead outline packages:

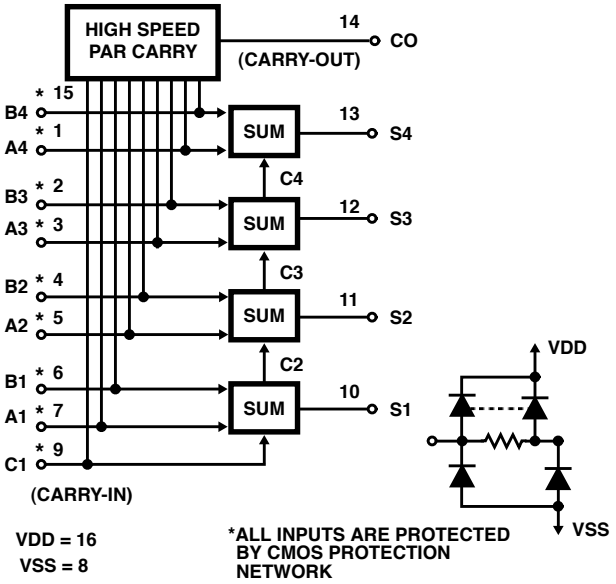
Braze Seal DIP	H4T
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

Pinout

CD4008BMS
TOP VIEW



Logic Diagram



TRUTH TABLE

A_i	B_i	C_i	C_O	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . .-0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . .±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	10	µA
				2	+125°C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Sum In to Sum Out	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	800	ns
			10, 11	+125°C, -55°C	-	1080	ns
Propagation Delay Carry In To Cum Out	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	740	ns
			10, 11	+125°C, -55°C	-	999	ns
Propagation Delay Sum In To Carry Out	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Carry In To Carry Out	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Sum In To Sum Out	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25°C	-	320	ns
		VDD = 15V	1, 2, 3	+25°C	-	230	ns
Propagation Delay Carry In To Sum Out	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25°C	-	310	ns
		VDD = 15V	1, 2, 3	+25°C	-	230	ns
Propagation Delay Sum In To Carry Out	TPLH3 TPHL3	VDD = 10V	1, 2, 3	+25°C	-	180	ns
		VDD = 15V	1, 2, 3	+25°C	-	130	ns
Propagation Delay Carry In To Carry Out	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	25	μA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10μA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10μA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0μA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	10 - 14	1 - 9, 15	16			
Static Burn-In 2 Note 1	10 - 14	8	1 - 7, 9, 15, 16			
Dynamic Burn-In Note 1	-	8	16	10 - 14	2, 4, 6, 15	1, 3, 5, 7, 9
Irradiation Note 2	10 - 14	8	1 - 7, 9, 15, 16			

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Typical Propagation Delay

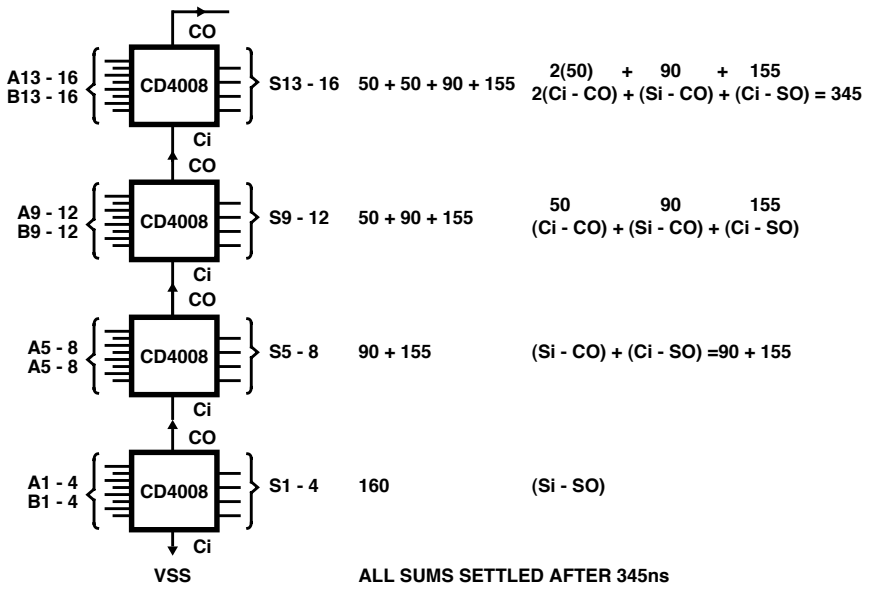


FIGURE 1. PROPAGATION DELAY FOR A 16 BIT ADDER (10V OPERATION)

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

Typical Performance Characteristics

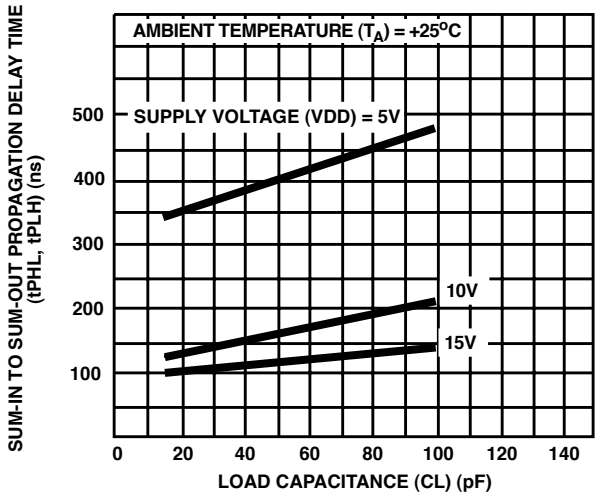


FIGURE 2. TYPICAL SUM-IN TO SUM-OUT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

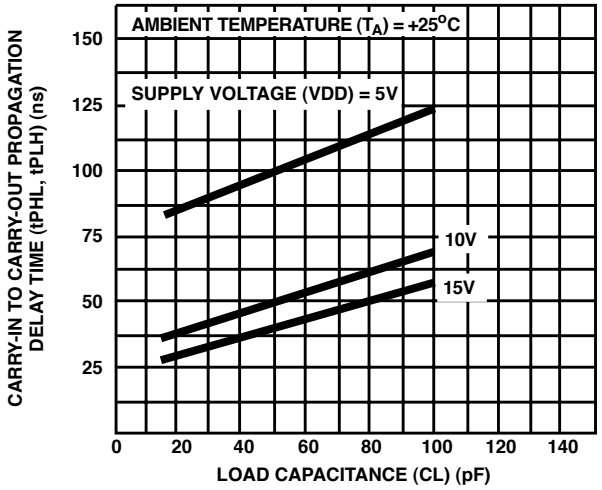


FIGURE 3. TYPICAL CARRY-IN TO CARRY-OUT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

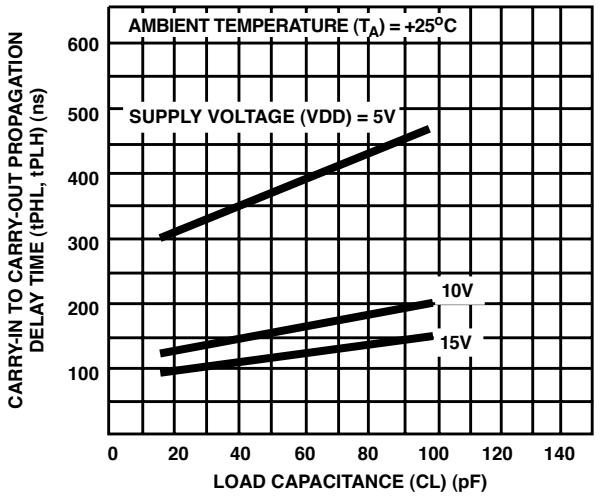


FIGURE 4. TYPICAL CARRY-IN TO SUM-OUT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

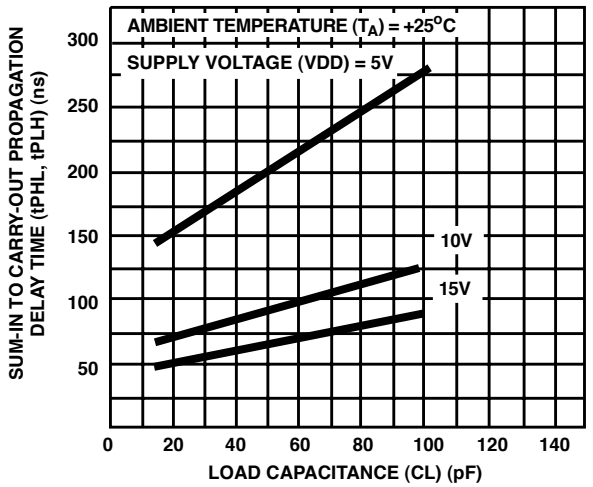


FIGURE 5. TYPICAL SUM-IN TO CARRY-OUT PROPAGATION DELAY TIME vs LOAD CAPACITANCE

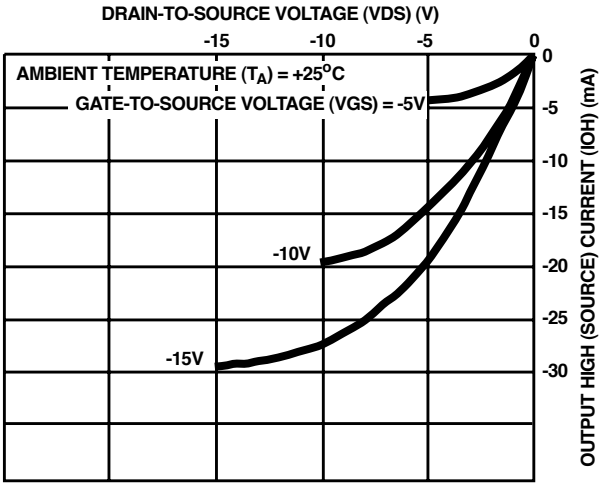


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

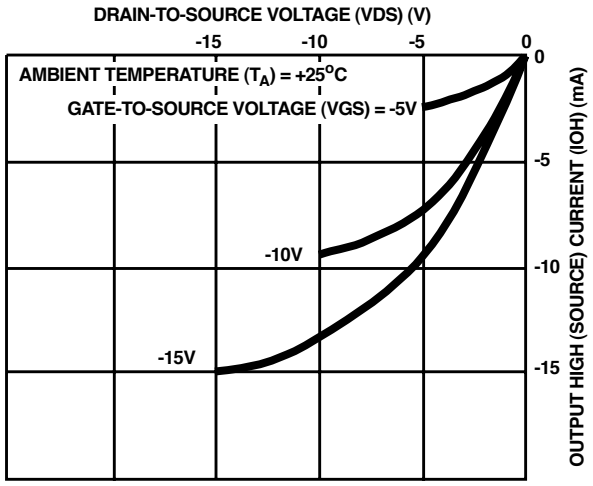


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

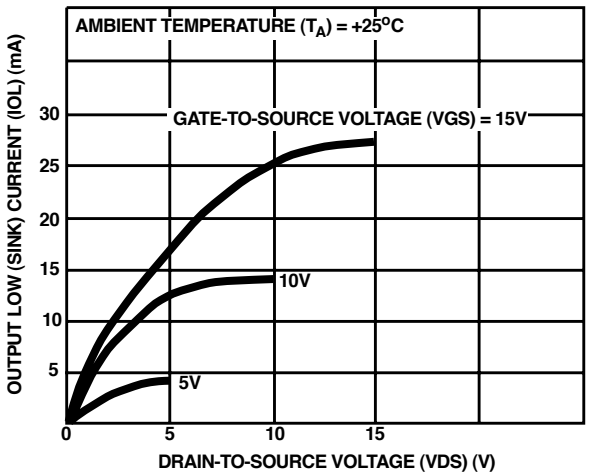


FIGURE 8. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

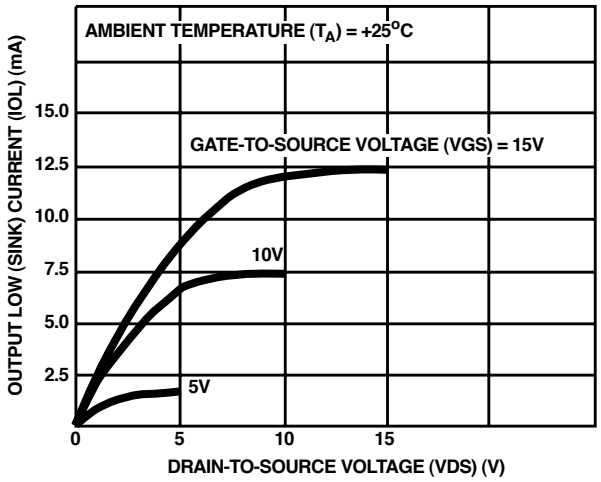


FIGURE 9. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

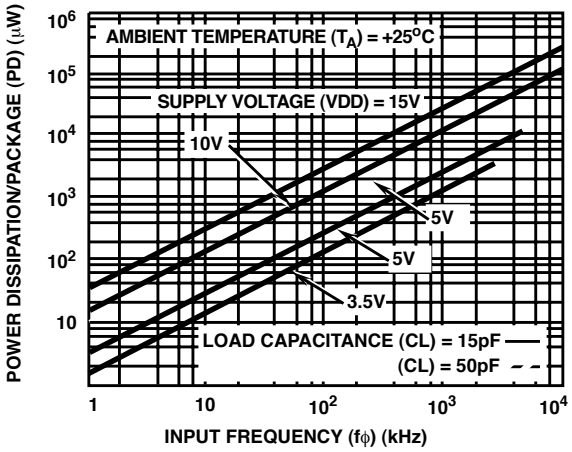
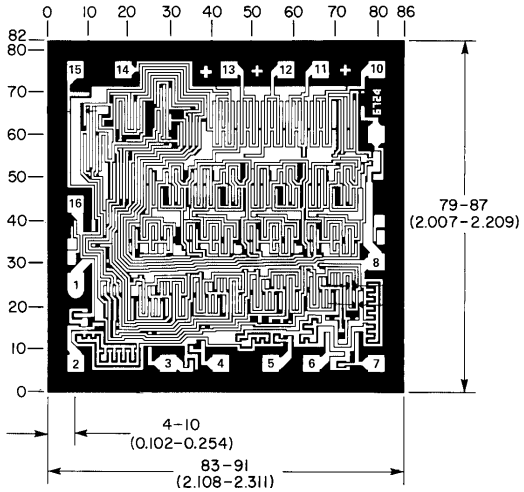


FIGURE 10. TYPICAL DISSIPATION CHARACTERISTICS

Chip Dimensions and Pad Layouts



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

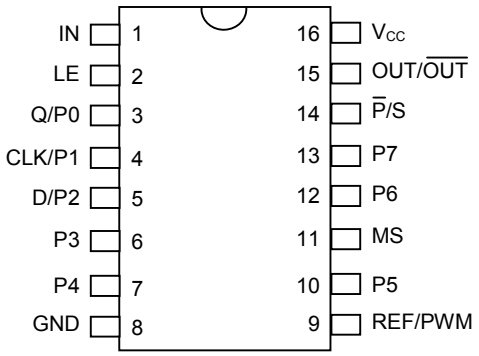
DS1023
8-Bit Programmable Timing Element

www.dalsemi.com

FEATURES

- Step sizes of 0.25 ns, 0.5 ns, 1 ns, 2 ns, 5 ns
- On-chip reference delay
- Configurable as delay line, pulse width modulator, or free-running oscillator
- Can delay clocks by a full period or more
- Guaranteed monotonicity
- Parallel or serial programming
- Single 5V supply
- 16-pin DIP or SOIC package

PIN ASSIGNMENT



DS1023 300-mil DIP
DS1023S 300-mil SOIC

PIN DESCRIPTION

IN	- Input
P0/Q	- Parallel Input P0 (parallel mode)
	- Serial Data Output (serial mode)
P1/CLK	- Parallel Input P1 (parallel mode)
	- Serial Input Clock (serial mode)
P2/D	- Parallel Input P2 (parallel mode)
	- Serial Data Input (serial mode)
P3 - P7	- Remaining Parallel Inputs
GND	- Ground
OUT/$\overline{\text{OUT}}$	- Output
REF/PWM	- Reference or PWM Output
$\overline{\text{P}}$/S	- Parallel / Serial Programming Select
MS	- Output Mode Select
LE	- Input Latch Enable
V_{CC}	- Supply Voltage

DESCRIPTION

The DS1023 is an 8-bit programmable delay line similar in function to the DS1020/DS1021.

Additional features have been added to extend the range of applications:

The internal delay line architecture has been revised to allow clock signals to be delayed by up to a full period or more. Combined with an on-chip reference delay (to offset the inherent or “step zero” delay of the device) clock phase can now be varied over the full 0-360 degree range.

On-chip gating is provided to allow the device to provide a pulse width modulated output, triggered by the input with duration set by the programmed value.

Alternatively the output signal may be inverted on chip, allowing the device to perform as a free-running oscillator if the output is (externally) connected to the input.

PROGRAMMING

The device programming is identical to the DS1020/DS1021. Note, however, that the serial clock and data pins are shared with three of the parallel input pins.

The $\overline{P}$/S pin controls the same function as "Mode Select" on the DS1020/DS1021 (but with reversed polarity). A low logic level on this pin enables the parallel programming mode. LE must be at a high logic level to alter the programmed value; when LE is taken low the data is latched internally and the parallel data inputs may be altered without affecting the programmed value. This is useful for multiplexed bus applications. For hard-wired applications LE should be tied to a high logic level.

When $\overline{P}$/S is high serial programming is enabled. LE must be held high to enable loading or reading of the internal register, during which time the delay is determined by the previously programmed value. Data is clocked in MSB to LSB order on the rising edge of the CLK input. Data transfer ends and the new value is activated when LE is taken low.

PARALLEL MODE ($\overline{P}$/S = 0)

In the PARALLEL programming mode, the output of the DS1023 will reproduce the logic state of the input after a delay determined by the state of the eight program input pins P0 - P7. The parallel inputs can be programmed using DC levels or computer-generated data. For infrequent modification of the delay value, jumpers may be used to connect the input pins to V_{CC} or ground. For applications requiring frequent timing adjustment, DIP switches may be used. The latch enable pin (LE) must be at a logic 1 in hardwired implementations.

Maximum flexibility is obtained when the eight parallel programming bits are set using computer-generated data. When the data setup (t_{DSE}) and data hold (t_{DHE}) requirements are observed, the enable pin can be used to latch data supplied on an 8-bit bus. Latch enable must be held at a logic 1 if it is not used to latch the data. After each change in delay value, a settling time (t_{EDV} or t_{PDV}) is required before input logic levels are accurately delayed.

SERIAL MODE ($\overline{P}$/S = 1)

In the SERIAL programming mode, the output of the DS1023 will reproduce the logic state of the input after a delay time determined by an 8-bit value clocked into serial port D. While observing data setup (t_{DSC}) and data hold (t_{DHC}) requirements, timing data is loaded in MSB-to-LSB order by the rising edge of the serial clock (CLK). The latch enable pin (LE) must be at a logic 1 to load or read the internal 8-bit input register, during which time the delay is determined by the last value activated. Data transfer ends and the new delay value is activated when latch enable (LE) returns to a logic 0. After each change, a settling time (t_{EDV}) is required before the delay is accurate.

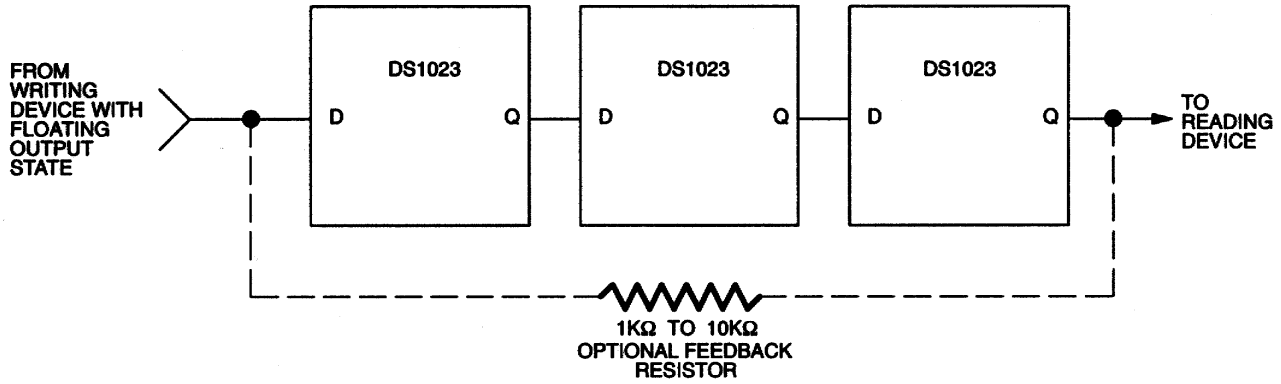
As timing values are shifted into the serial data input (D), the previous contents of the 8-bit input register are shifted out of the serial output pin (Q) in MSB-to-LSB order. By connecting the serial output of one DS1023 to the serial input of a second DS1023, multiple devices can be daisy-chained (cascaded) for programming purposes (Figure 1). The total number of serial bits must be eight times the number of units daisy-chained and each group of 8 bits must be sent in MSB-to-LSB order.

Applications can read the setting of the DS1023 Delay Line by connecting the serial output pin (Q) to the serial input (D) through a resistor with a value of 1 to 10 kohms (Figure 2). Since the read process is destructive, the resistor restores the value read and provides isolation when writing to the device. The resistor must connect the serial output (Q) of the last device to the serial input (D) of the first device of a daisy chain (Figure 1). For serial readout with automatic restoration through a resistor, the device used to write serial data must go to a high impedance state.

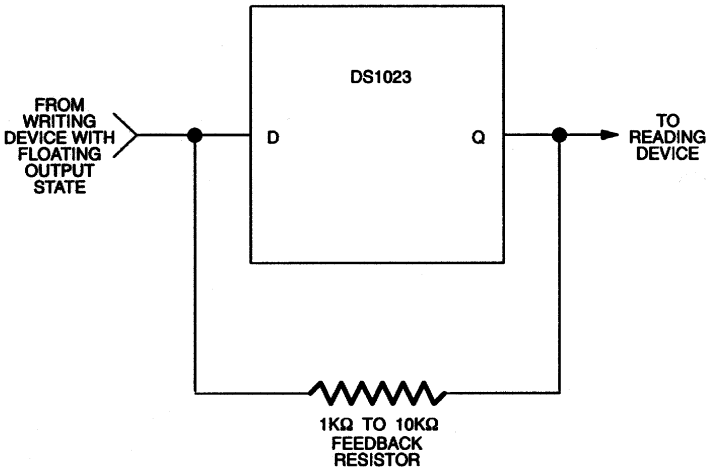
To initiate a serial read, latch enable (LE) is taken to a logic 1 while serial clock (CLK) is at a logic 0. After a waiting time (t_{EQV}), bit 7 (MSB) appears on the serial output (Q). On the first rising (0 --> 1) transition of the serial clock (CLK), bit 7 (MSB) is rewritten and bit 6 appears on the output after a time t_{CQV}. To restore the input register to its original state, this clocking process must be repeated eight times. In the case of a daisy chain, the process must be repeated eight times per package. If the value read is restored before latch enable (LE) is returned to logic 0, no settling time (t_{EDV}) is required and the programmed delay remains unchanged.

Since the DS1023 is a CMOS design, unused input pins (P3 - P7) must be connected to well-defined logic levels; they must not be allowed to float. Serial output Q/P0 should be allowed to float if unused.

CASCADING MULTIPLE DEVICES (DAISY CHAIN) Figure 1



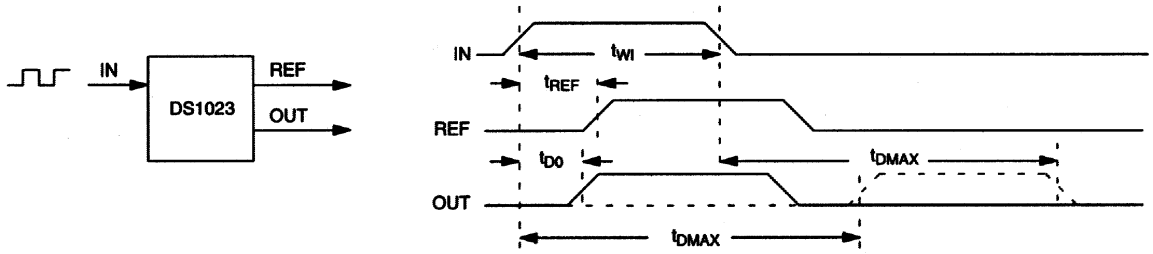
SERIAL READOUT Figure 2



REFERENCE DELAY

In all delay lines there is an inherent, or “step zero”, delay caused by the propagation delay through the input and output buffers. In this device the step zero delay can be quite large compared to the delay step size. To simplify system design a reference delay has been included on chip which may be used to compensate for the step zero delay. In practice this means that if the device is supplied with a clock, for example, the minimum programmed output delay is effectively zero with respect to the reference delay.

For highest accuracy it is strongly recommended that the reference delay is used. Variations in input voltage levels and transition times can significantly alter the measured delay from input to output. This effect is totally removed if the reference delay output is used. Furthermore, adverse effects on step zero delay caused by process temperature coefficients are also cancelled out.



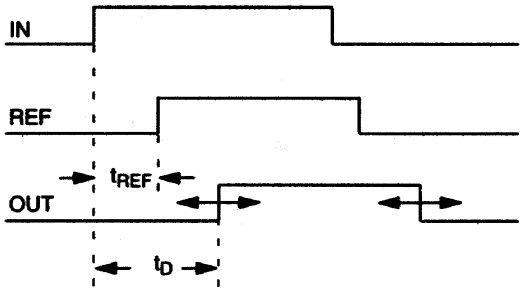
INPUT PULSE DURATION

The internal architecture of the DS1023 allows the output delay time to be considerably longer than the input pulse width (see ac specifications). This feature is useful in many applications, in particular clock phase control where delays up to and beyond one full clock period can be achieved.

MODE SELECT

The DS1023 has four possible output functions but only two output pins. The functionality of the two output pins is determined by the Mode Select (MS) pin.

MS = 0 Figure 3

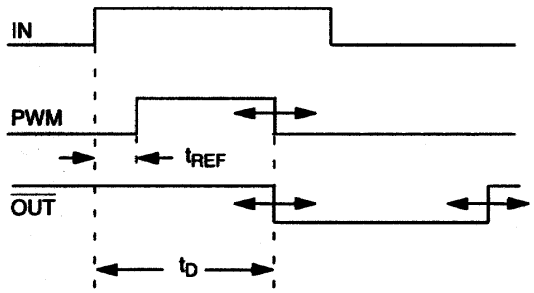


Output Function	**Name**	**Pin Number**
Reference Output	REF	9
Delayed Output	OUT	15

OUT is a copy of the input waveform that is delayed by an amount set by the programmed values (Table 1). A programmed value of zero will still result in a non-zero delay as indicated in the Step Zero delay specification. The signal on OUT is the same polarity as the input.

REF is a fixed reference delay. It also is a copy of the input waveform but the delay interval is fixed to a value approximately equal to the Step Zero Value of the device (as shown in the Reference Delay specification). In fact the device is trimmed to ensure that the Reference Delay is always slightly longer than the Step Zero Value (by 1.5 ns typically).

MS = 1 Figure 4

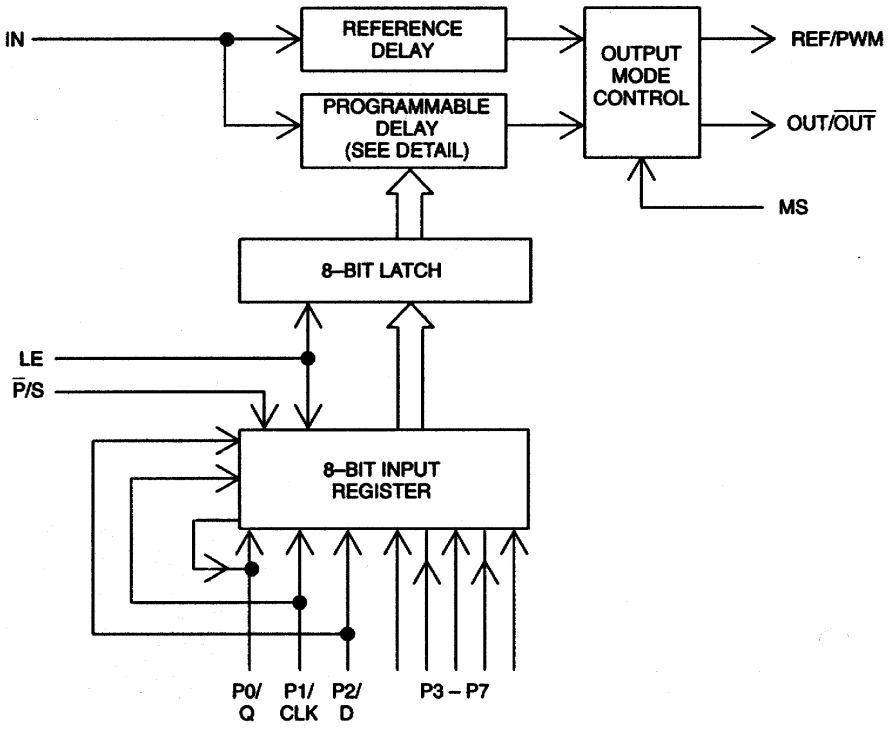


Output Function	**Name**	**Pin Number**
Pulse Width Modulated Output	PWM	9
Delayed and Inverted Output	$\overline{\text{OUT}}$	15

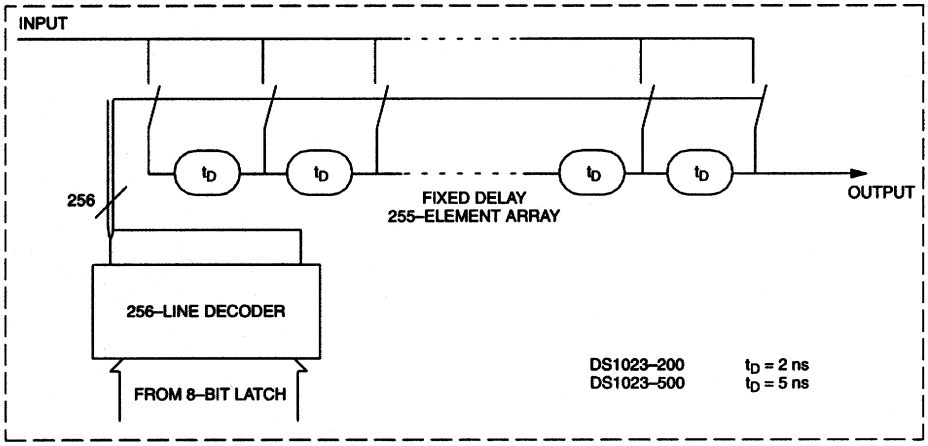
PWM is an output triggered by the rising edge of the input waveform. After a time interval approximately equal to the Step Zero delay of the device the PWM output will go high. The output will return to a low level after a time interval determined by the programmed values (Table 1). Hence output pulse widths can be obtained from (nearly) zero to the full delay range of the device. In practice the minimum output pulse width is limited by the response time of the device to approximately 5ns. Programmed values less than this will result in degradation of the output high level voltage until ultimately no discernible output pulse is produced. The frequency/repetition rate of the output is determined by the input frequency. The input pulse width can be shorter than the output pulse width, and is limited only by the minimum input pulse width specification. The PWM function is not "re-triggerable", subsequent input trigger pulses should not be present until the output has returned to a low level.

$\overline{\text{OUT}}$ is an inverted copy of the input waveform that is delayed by an amount set by the programmed values (Table 1). A programmed value of zero will still result in a non-zero delay as indicated in the Step Zero delay specification. The $\overline{\text{OUT}}$ pin may also be externally connected to the input pin to produce a free-running oscillator. The frequency of oscillation is determined by the programmed delay value of the device (see Table 2).

FUNCTIONAL BLOCK DIAGRAM Figure 5

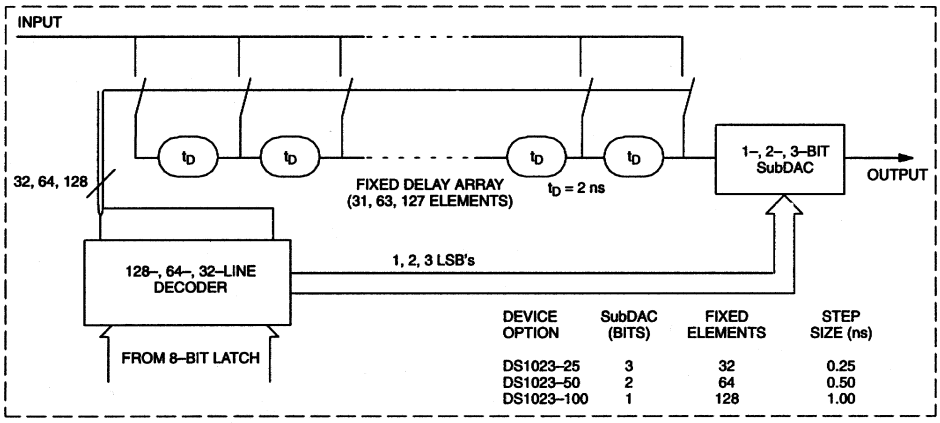


DELAY LINE DETAIL (CONCEPTUAL) - DS1023-200, DS1023-500 Figure 6



DELAY LINE DETAIL (CONCEPTUAL) - DS1023-25, DS1023-50, DS1023-100

Figure 7



PART NUMBER TABLE Table 1

DELAYS RANGES AND TOLERANCE (all times measured in ns)					
PART NUMBER	STEP SIZE	MAX. DELAY TIME (1)/ MAX. OUTPUT PULSE WIDTH (2)	MAXIMUM DEVIATION (3)	MAXIMUM I/P FREQ	MINIMUM I/P PULSE WIDTH
DS1023-025	0.25	63.75	±1	25 MHz	20
DS1023-050	0.50	127.5	±2	25 MHz	20
DS1023-100	1.0	255	±4	25 MHz	20
DS1023-200	2.0	510	±8	25 MHz	20
DS1023-500	5.0	1275	±20	10 MHz	50

1. In "Normal" mode (MS=0). Measured with respect to REF output. The minimum delay time is zero (or less, by 1.5 ns typically)

2. In PWM mode (MS=1). The minimum output pulse width for reliable operation is 5 ns; programmed values less than this may produce reduced output voltage levels or no output at all.

3. This is the deviation from a straight line drawn between the step zero value and the maximum programmed delay time.

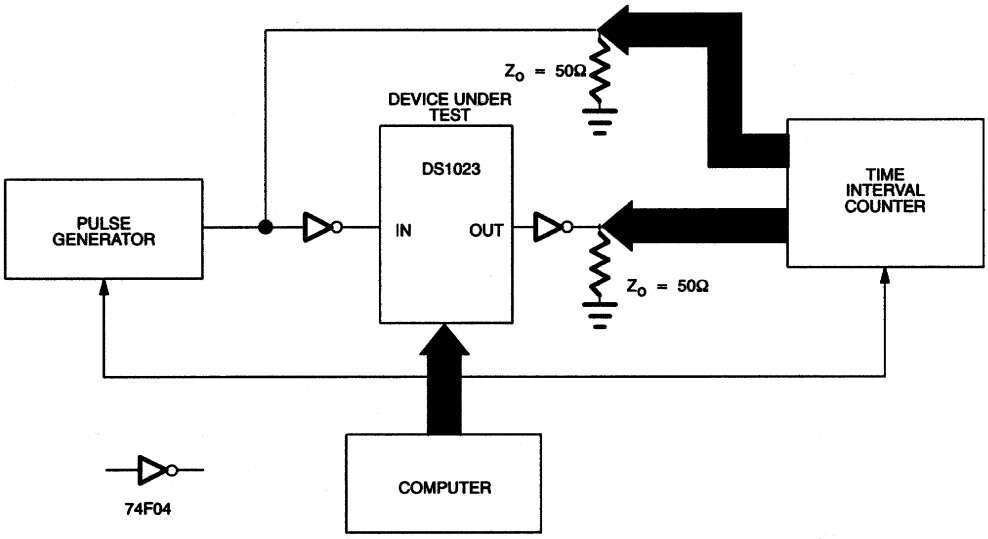
OSCILLATOR CONFIGURATION Table 2

PART NUMBER	STEP SIZE (4)	MINIMUM O/P FREQUENCY (5)	MAXIMUM O/P FREQUENCY (5)
DS1023-025	0.5	6.6 MHz	22 MHz
DS1023-050	1.0	3.6 MHz	22 MHz
DS1023-100	2.0	1.9 MHz	22 MHz
DS1023-200	4.0	0.98 MHz	22 MHz
DS1023-500	10.0	0.4 MHz	22 MHz

4. Step size in output period (in ns).

5. Maximum output frequency depends on the actual step zero delay value, worst case values are shown in the table. The output period is given by: 2 * t_D where: t_D = absolute delay value.

DALLAS SEMICONDUCTOR TEST CIRCUIT Figure 8



TEST SETUP DESCRIPTION

Figure 8 illustrates the hardware configuration used for measuring the timing parameters of the DS1023. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1023 serial and parallel ports are controlled by interfaces to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

TEST CONDITIONS

INPUT:

Ambient Temperature:	25°C ± 3°C
Supply Voltage (V_{CC}):	5.0V ± 0.1V
Input Pulse:	High = 3.0V ± 0.1V
	Low = 0.0V ± 0.1V
Source Impedance:	50 ohms max.
Rise and Fall Time:	3.0 ns max. (measured between 0.6V and 2.4V)
Pulse Width:	500 ns
Period:	1 μs

NOTE: Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

OUTPUT:

Output is loaded with a 74F04. Delay is measured between the 1.5V level of the rising edge of the input signal and the 1.5V level of the corresponding edge of the output.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin	-1.0V to +7.0V
Operating Temperature Range	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds
Short Circuit Output Current	50 mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

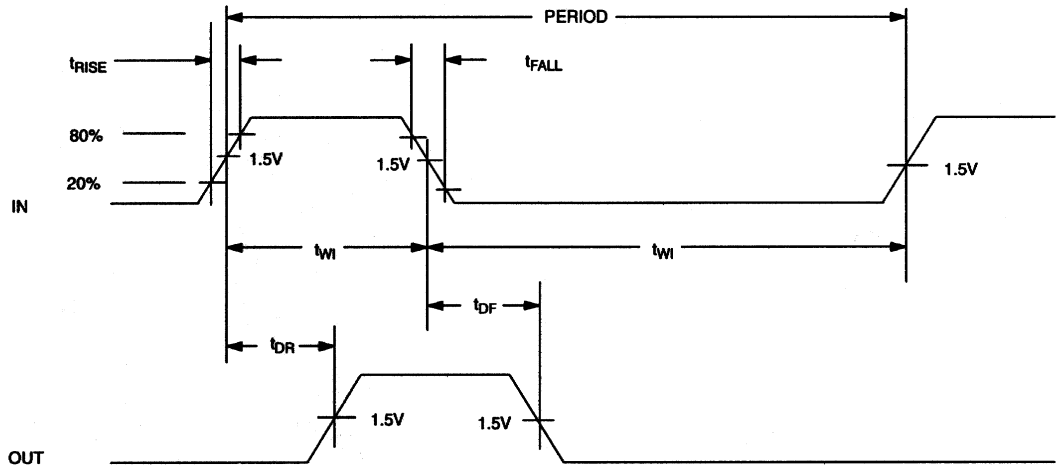
DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.75	5	5.25	V	
High Level Input Voltage	V_{IH}	2		V_{CC} +0.5	V	
Low Level Input Voltage	V_{IL}	-0.5		0.8	V	
Input Leakage Current ($0<V_I<V_{CC}$)	I_I	-1		+1	µA	
Active Current	I_{CC}		30	60	mA	
High Level Output Current (V_{CC} = Min, V_{OH} = 2.7V)	I_{OH}			-1	mA	
Low Level Output Current (V_{CC} = Min, V_{OL} = 0.5V)						
-Q output	I_{OL}	4			mA	
-All other outputs	I_{OL}	8			mA	

AC ELECTRICAL CHARACTERISTICS - CONTROL/INTERFACE SPECIFICATIONS ALL SPEED OPTIONS (T_A= 0°C to 70°C; V_{CC}= 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Serial Clock Frequency	f_{CLK}			10	MHz	
Input Pulse Width (LE, CLK)	t_W	50			ns	
Data Setup to Clock	t_{DSC}	30			ns	
Data Hold from Clock	t_{DHC}	0			ns	
Data Setup to Enable	t_{DSE}	30			ns	
Data Hold from Enable	t_{DHE}	0			ns	
Enable Setup to Clock	t_{ES}	0			ns	
Enable Hold from Clock	t_{EH}	30			ns	
LE to Q Valid	t_{EQV}			50	ns	
LE to Q Hi-Z	t_{EQZ}	0		50	ns	
CLK to Q Valid	t_{CQV}			50	ns	
CLK to Q Invalid	t_{CQX}	0			ns	
Parallel Input to Delay Valid	t_{PDV}			500	ns	
Parallel Input to Delay Invalid	t_{PDX}	0			ns	
LE to Delay Valid	t_{EDV}			500	ns	
LE to Delay Invalid	t_{EDX}	0			ns	
Power Up Time	t_{PU}			100	ms	

TIMING DIAGRAM: SILICON DELAY LINE Figure 9



AC ELECTRICAL CHARACTERISTICS - DS1023-025 Delay Specifications (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Step Zero Delay -absolute -wrt REF	 t_{D0} t_{DREF0}	 -2	 16.5 -1.5	 22 0	 ns ns	 1, 13 2, 14
Reference Delay	t_{REF}		18	22	ns	3, 13
Delay Step Size	t_{STEP}	0	0.25	0.75	ns	4
Maximum Delay -absolute -wrt REF	 t_{DMAX} t_{DREF}	 75 60	 80 63.75	 89 67.5	 ns ns	 5, 13 6, 14
Delay Matching, Rising Edge to Falling Edge		-1		+1	ns	15
Integral Non-linearity (deviation from straight line)	t_{err}	-1	0	+1	ns	7
$\overline{OUT}$ Delta Delay	t_{INV0}	0	1	2	ns	8
IN High to PWM High	t_{PWM0}		16.5	22	ns	9, 13
Minimum PWM Output Pulse Width	t_{PWM}	5			ns	10
Minimum Input Pulse Width	t_{WI}	20			ns	11
Minimum Input Period		40			ns	12
Input Rise and Fall Times	t_r, t_f	0		1	µs	16

AC ELECTRICAL CHARACTERISTICS – DS1023-050 Delay Specifications (T_A= 0°C to 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Step Zero Delay -absolute -wrt REF	 t_{D0} t_{DREF0}	 -2	 16.5 -1.5	 22 0	 ns ns	 1, 13 2, 14
Reference Delay	t_{REF}		18	22	ns	3, 13
Delay Step Size	t_{STEP}	0	0.5	1.5	ns	4
Maximum Delay -absolute -wrt REF	 t_{DMAX} t_{DREF}	 139 123	 144 127.5	 154 132	 ns ns	 5, 13 6, 14
Delay Matching, Rising Edge to Falling Edge		-1		+1	ns	15
Integral Non-linearity (deviation from straight line)	t_{err}	-2	0	+2	ns	7
$\overline{OUT}$ Delta Delay	t_{INV0}	0	1	2	ns	8
IN High to PWM High	t_{PWM0}		16.5	22	ns	9, 13
Minimum PWM Output Pulse Width	t_{PWM}	5			ns	10
Minimum Input Pulse Width	t_{WI}	20			ns	11
Minimum Input Period		40			ns	12
Input Rise and Fall Times	t_r, t_f	0		1	µs	16

AC ELECTRICAL CHARACTERISTICS – DS1023-100 Delay Specifications (T_A = 0°C – 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Step Zero Delay -absolute -wrt REF	 t_{D0} t_{DREF0}	 -2	 16.5 -1.5	 22 0	 ns ns	 1, 13 2, 14
Reference Delay	t_{REF}		18	22	ns	3, 13
Delay Step Size	t_{STEP}	0	1	1.5	ns	4
Maximum Delay -absolute -wrt REF	 t_{DMAX} t_{DREF}	 262 247	 272 255	 285 263	 ns ns	 5, 13 6, 14
Delay Matching, Rising Edge to Falling Edge		-1		+1	ns	15
Integral Non-linearity (deviation from straight line)	t_{err}	-4	0	+4	ns	7
$\overline{OUT}$ Delta Delay	t_{INV0}	0	1	2	ns	8
IN High to PWM High	t_{PWM0}		16.5	22	ns	9, 13
Minimum PWM Output Pulse Width	t_{PWM}	5			ns	10
Minimum Input Pulse Width	t_{WI}	20			ns	11
Minimum Input Period		40			ns	12
Input Rise and Fall Times	t_r, t_f	0		1	µs	16

AC ELECTRICAL CHARACTERISTICS - DS1023-200 Delay Specifications (T_A = 0°C - 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Step Zero Delay -absolute -wrt REF	 t_{D0} t_{DREF0}	 -2	 16.5 -1.5	 22 0	 ns ns	 1, 13 2, 14
Reference Delay	t_{REF}		18	22	ns	3, 13
Delay Step Size	t_{STEP}	1.5	2	2.5	ns	
Maximum Delay -absolute -wrt REF	 t_{DMAX} t_{DREF}	 509 494	 527 510	 548 526	 ns ns	 5, 13 6, 14
Delay Matching, Rising Edge to Falling Edge		-1		+1	ns	15
Integral Non- linearity (deviation from straight line)	t_{err}	-8	0	+8	ns	7
$\overline{OUT}$ Delta Delay	t_{INV0}	0	1	2	ns	8
IN High to PWM High	t_{PWM0}		16.5	22	ns	9, 13
Minimum PWM Output Pulse Width	t_{PWM}	5			ns	10
Minimum Input Pulse Width	t_{WI}	20			ns	11
Minimum Input Period		40			ns	12
Input Rise and Fall Times	t_r, t_f	0		1	µs	16

AC ELECTRICAL CHARACTERISTICS – DS1023-500 Delay Specifications (T_A = 0°C – 70°C; V_{CC} = 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Step Zero Delay -absolute -wrt REF	 t_{D0} t_{DREF0}	 -2	 16.5 -1.5	 22 0	 ns ns	 1, 13 2, 14
Reference Delay	t_{REF}		18	22	ns	3, 13
Delay Step Size	t_{STEP}	4	5	6	ns	
Maximum Delay -absolute -wrt REF	 t_{DMAX} t_{DREF}	 1250 1235	 1292 1275	 1337 1315	 ns ns	 5, 13 6, 14
Delay Matching, Rising Edge to Falling Edge		-1		+1	ns	15
Integral Non- linearity (deviation from straight line)	t_{err}	-20	0	+20	ns	7
$\overline{OUT}$ Delta Delay	t_{INV0}	0	1	2	ns	8
IN High to PWM High	t_{PWM0}		16.5	22	ns	9, 13
Minimum PWM Output Pulse Width	t_{PWM}	5			ns	10
Minimum Input Pulse Width	t_{WI}	50			ns	11
Minimum Input Period		100			ns	12
Input Rise and Fall Times	t_r, t_f	0		1	µs	16

NOTES:

1. Delay from input to output with a programmed delay value of zero.

2. This is the relative delay between REF and OUT. The device is trimmed such that when programmed to zero delay the OUT output will always appear before the REF output. This parameter is numerically equal to t_{D0}-t_{REF}. (See Figure 15).

3. The reference delay is closely matched to the step zero delay to allow relative timings down to zero or less.

4. This is the worst case condition when the SubDAC switches from its maximum to minimum value. All other steps are ±0.5 lsb. This comment does not apply to -200 and -500 devices which do not use a SubDAC. (See Figure 14)

5. This is the actual measured delay from IN to OUT. This parameter will exhibit greater temperature variation than the relative delay parameter.

6. This is the actual measured delay with respect to the REF output. This parameter more closely reflects the programmed delay value than the absolute delay parameter. (See Figure 15).

7. This is the maximum deviation from a straight line response drawn between the step zero delay and the maximum programmed delay. Therefore it is indicative of the maximum error in the measured delay versus the programmed delay with respect to the REF output. The absolute delay measurement from IN to OUT will in addition have an offset error equal to the step zero delay and its tolerance. (See Figure 13).

8. Change in delay value when the inverted output is selected instead of the normal, non-inverting, output.

9. In PWM mode the delay between the rising edge of the input and the rising edge of the output.

10. The minimum value for which the PWM pulse width should be programmed. Narrower pulse widths may be programmed but output levels may be impaired and ultimately no output pulse will be produced.

11. This is the minimum allowable interval between transitions on the input to assure accurate device operation. This parameter may be violated but timing accuracy may be impaired and ultimately very narrow pulse widths will result in no output from the device.

12. This parameter applies to normal delay mode only. When a 50% duty cycle input clock is used this defines the highest usable clock frequency. When asymmetrical clock inputs are used the maximum usable clock frequency must be reduced to conform to the minimum input pulse width requirement. In PWM mode the minimum input period is equal to the step zero delay and the programmed delay ($t_{DO} + t_D$).

13. Measured from rising edge of the input to the rising edge of the output (t_{DR}).

14. From rising edge to rising edge.

15. This is the difference in measured delay between rising edge (input to output), t_{DR} and falling edges (input to output), t_{DF}.

16. Faster rise and fall times will give the greatest accuracy in measured delay. Slow edges (outside the specification maximum) may result in erratic operations.

TERMINOLOGY

Period: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

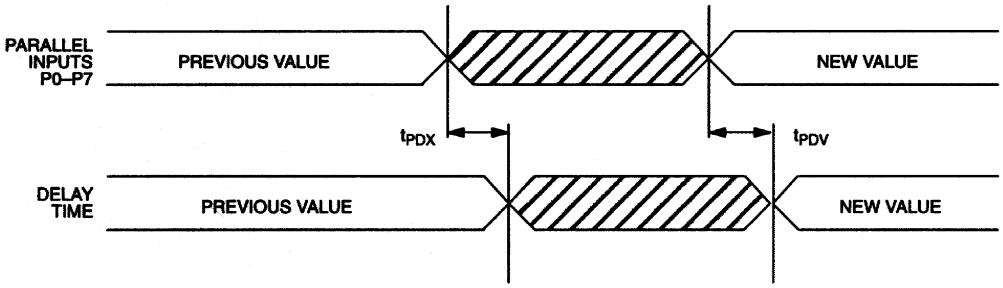
t_{WI} (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V point on the leading edge.

t_{RISE} (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

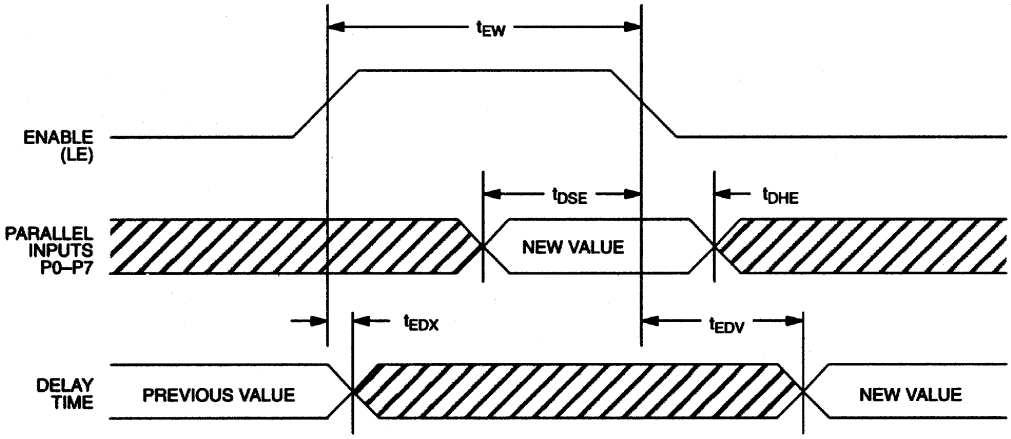
t_{FALL} (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t_D (Time Delay): The elapsed time between the 1.5V point on the edge of an input pulse and the 1.5V point on the corresponding edge of the output pulse.

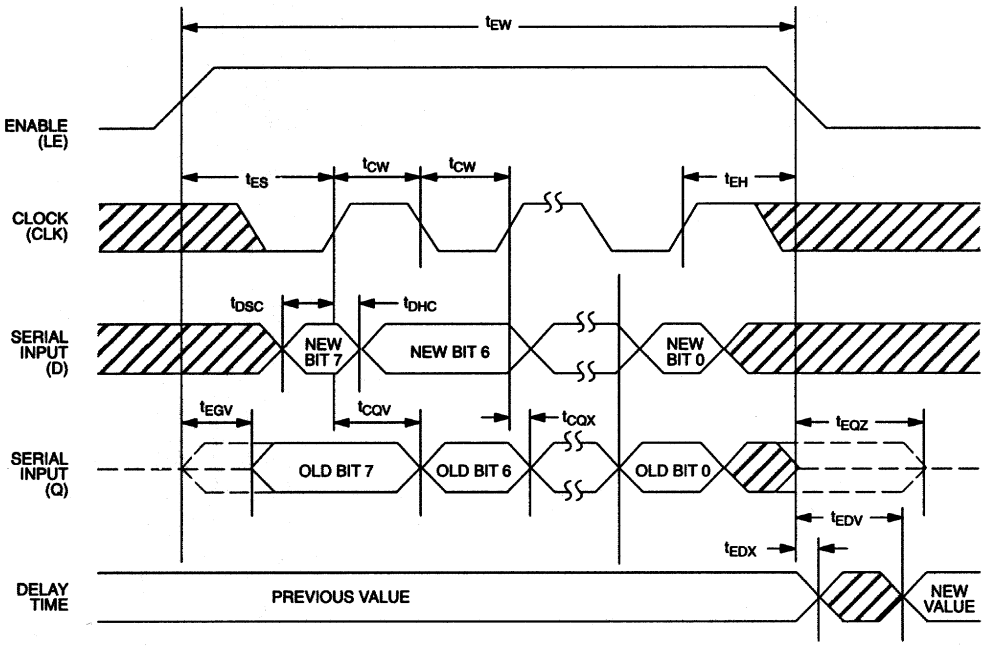
TIMING DIAGRAM: NON-LATCHED PARALLEL MODE ($\overline{P}$/S = 0, LE = 1) Figure 10



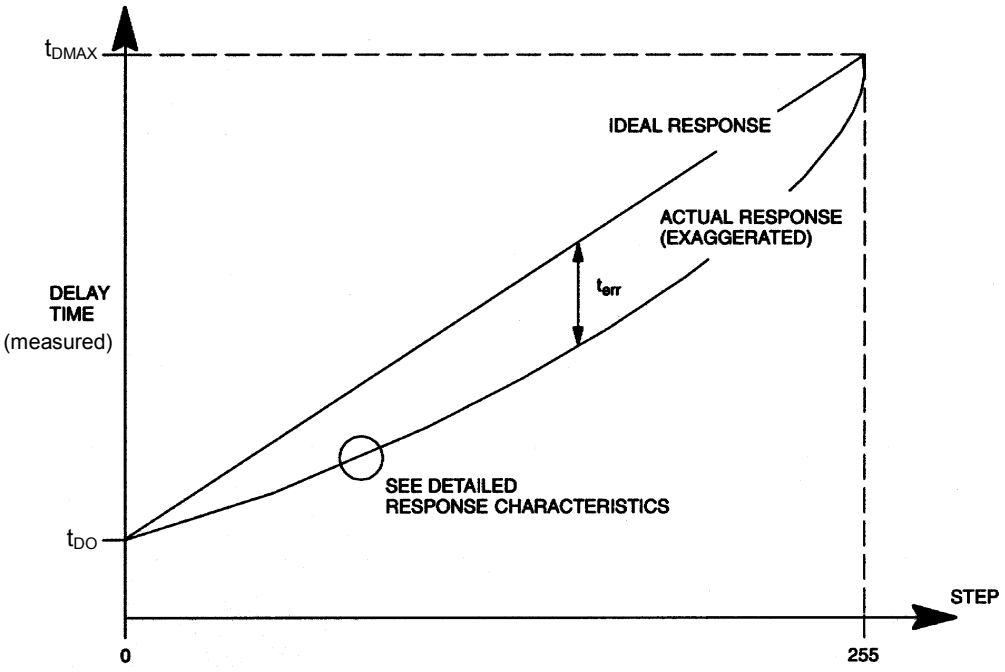
TIMING DIAGRAM: LATCHED PARALLEL MODE ($\overline{P}$/S = 0) Figure 11



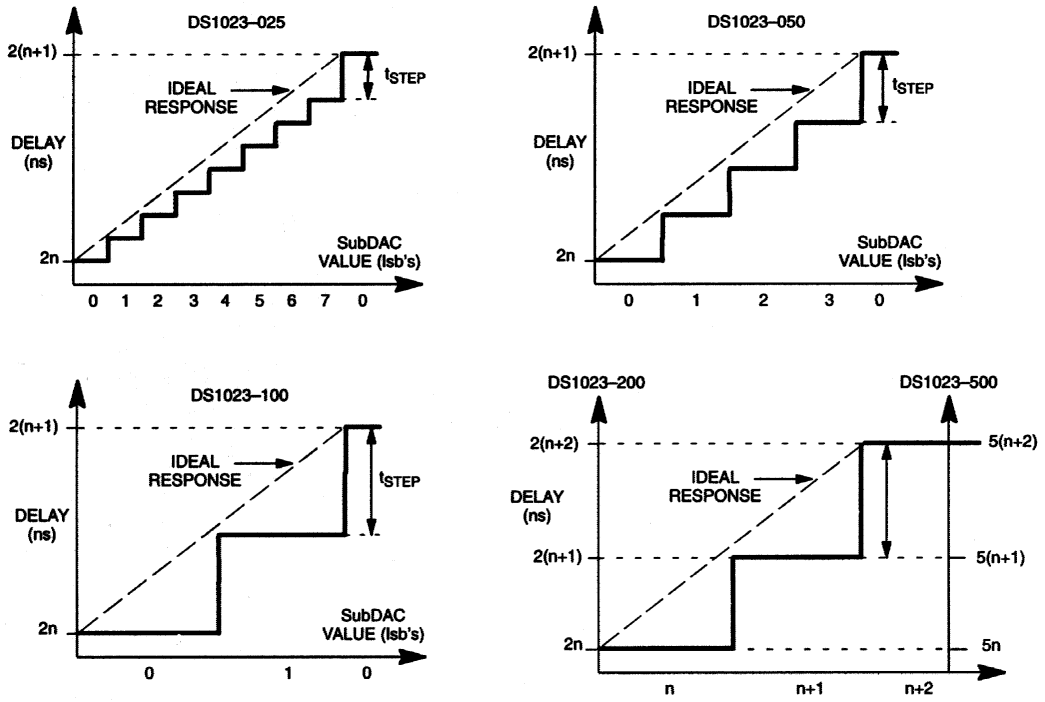
TIMING DIAGRAM: SERIAL MODE ($\overline{P}$/S = 1) Figure 12



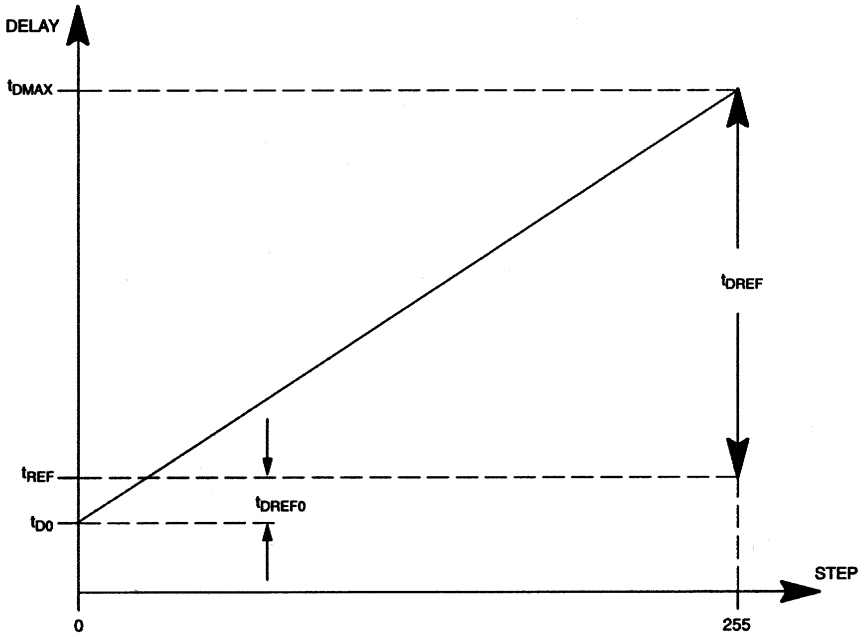
DELAY vs PROGRAMMED VALUE Figure 13



DETAILED RESPONSE CHARACTERISTICS Figure 14



DELAY PARAMETERS Figure 15



NOTES:

1. The device is trimmed such that $t_{DREF} = 255 *$ (nominal step size).

2. Since t_{DO} is trimmed to be less than t_{REF}, the actual step size will be slightly above the nominal value.

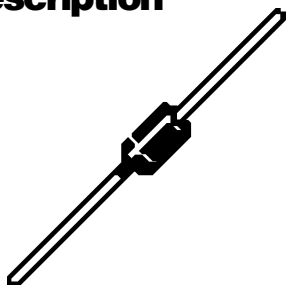
3. Consequently the range of absolute delay values (t_{DMAX}-t_{DO}) will also exceed the nominal range by an amount equal to t_{DREF0}.

FCI Semiconductor *Data Sheet*

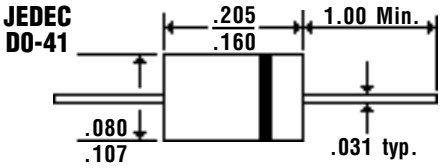
1.0 Amp SCHOTTKY BARRIER RECTIFIERS

1N5817, 18 & 19 Series

Description



Mechanical Dimensions

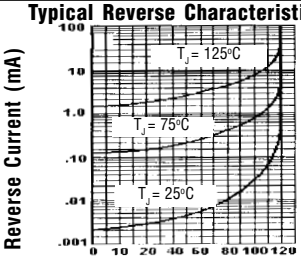


Features

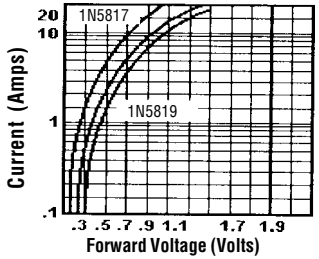
- **EXTREMELY LOW V_F**
- **LOW POWER LOSS — HIGH EFFICIENCY**
- **LOW STORED CHARGE; MAJORITY CARRIER CONDUCTION**
- **MEETS UL SPECIFICATION 94V-0**

Electrical Characteristics @ 25°C.	***IN5817, 18 & 19 Series***			**Units**
Maximum Ratings	**IN5817**	**IN5818**	**IN5819**	
Peak Repetitive Reverse Voltage...V_{RRM}	20	30	40	Volts
Working Peak Reverse Voltage...V_{RWM}	20	30	40	Volts
DC Blocking Voltage...V_{DC}	20	30	40	Volts
RMS Reverse Voltage...$V_{R(rms)}$	14	21	28	Volts
Average Forward Rectified Current...$I_{F(av)}$ @ T_A = 55°C	.....	1.0	.....	Amps
Non-Repetitive Peak Forward Surge Current...I_{FSM} @ Rated Load Conditions, ½ Wave, 60 HZ, T_J = 75°C	.....	25	.....	Amps
Forward Voltage...V_F @ I_F = 3.0 Amps	.450	.550	.600	Volts
DC Reverse Current...I_R @ Rated DC Blocking Voltage T_J = 25°C	.....	1.0	.....	mAmps
T_J = 100°C	.....	10	.....	mAmps
Typical Junction Capacitance...C_J	110	<	.70 ..... >	pF
Operating & Storage Temperature Range...T_J, T_{STRG}	.....	-65 to 125	.....	°C

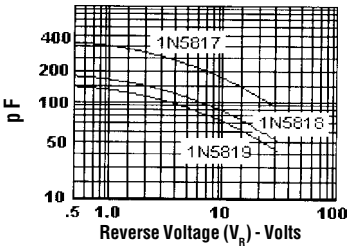
Typical Reverse Characteristics



Instantaneous Forward Characteristics



Typical Junction Capacitance



19-0269; Rev 0; 9/94

MAXIM

5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulators

MAX603/MAX604

General Description

The MAX603/MAX604 low-dropout, low quiescent current, linear regulators supply 5V, 3.3V, or an adjustable output for currents up to 500mA. They are available in a 1.8W SO package. Typical dropouts are 320mV at 5V and 500mA, or 240mV at 3.3V and 200mA. Quiescent currents are 15µA typ and 35µA max. Shutdown turns off all circuitry and puts the regulator in a 2µA off mode. A unique protection scheme limits reverse currents when the input voltage falls below the output. Other features include foldback current limiting and thermal overload protection.

The output is preset at 3.3V for the MAX604 and 5V for the MAX603. In addition, both devices employ Dual Mode™ operation, allowing user-adjustable outputs from 1.25V to 11V using external resistors. The input voltage supply range is 2.7V to 11.5V.

The MAX603/MAX604 feature a 500mA P-channel MOSFET pass transistor. This transistor allows the devices to draw less than 35µA over temperature, independent of the output current. The supply current remains low because the P-channel MOSFET pass transistor draws no base currents (unlike the PNP transistors of conventional bipolar linear regulators). Also, when the input-to-output voltage differential becomes small, the internal P-channel MOSFET does not suffer from excessive base current losses that occur with saturated PNP transistors.

Applications

5V and 3.3V Regulators
1.25V to 11V Adjustable Regulators
Battery-Powered Devices
Pagers and Cellular Phones
Portable Instruments
Solar-Powered Instruments

Features

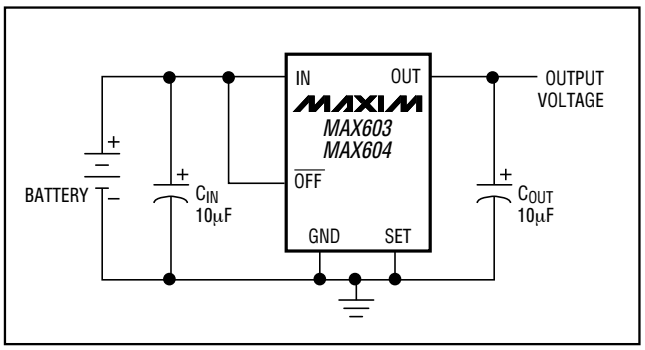
- **500mA Output Current, with Foldback Current Limiting**
- **High-Power (1.8W) 8-Pin SO Package**
- **Dual Mode™ Operation: Fixed or Adjustable Output from 1.25V to 11V**
- **Large Input Range (2.7V to 11.5V)**
- **Internal 500mA P-Channel Pass Transistor**
- **15µA Typical Quiescent Current**
- **2µA (Max) Shutdown Mode**
- **Thermal Overload Protection**
- **Reverse-Current Protection**

Ordering Information

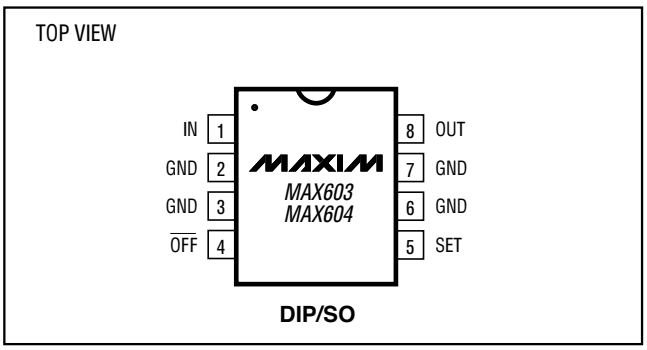
PART	TEMP. RANGE	PIN-PACKAGE
MAX603CPA	0°C to +70°C	8 Plastic DIP
MAX603CSA	0°C to +70°C	8 SO
MAX603C/D	0°C to +70°C	Dice*
MAX603EPA	-40°C to +85°C	8 Plastic DIP
MAX603ESA	-40°C to +85°C	8 SO
MAX603MJA	-55°C to +125°C	8 CERDIP**
MAX604CPA	0°C to +70°C	8 Plastic DIP
MAX604CSA	0°C to +70°C	8 SO
MAX604C/D	0°C to +70°C	Dice*
MAX604EPA	-40°C to +85°C	8 Plastic DIP
MAX604ESA	-40°C to +85°C	8 SO
MAX604MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C, DC parameters only.*
*** Contact factory for availability.*

Typical Operating Circuit



Pin Configuration



™ Dual Mode is a trademark of Maxim Integrated Products.

5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IN or OUT to GND).....-0.3V to +12V
Output Short-Circuit Duration .....1 min
Continuous Output Current.....600mA
SET, $\overline{OFF}$ Input Voltages .....-0.3V to the greater of (IN + 0.3V) or (OUT + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 23.6mW/°C above +70°C).....1.8W
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX60_C_A .....0°C to +70°C
MAX60_E_A .....-40°C to +85°C
MAX60_MJA .....-55°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 6V (MAX603) or 4.3V (MAX604), C_{IN} = C_{OUT} = 10µF, $\overline{OFF}$ = V_{IN}, SET = GND, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	SET = OUT, R_L = 1kΩ	MAX60_C	2.7		11.5	V
			MAX60_E	2.9		11.5	
			MAX60_M	3.0		11.5	
Output Voltage (Note 2)	V_{OUT}	I_{OUT} = 20µA to 500mA, 6.0V < V_{IN} < 11.5V	MAX603	4.75	5.00	5.25	V
		I_{OUT} = 20µA to 300mA, 4.3V < V_{IN} < 11.5V	MAX604	3.15	3.30	3.45	
Load Regulation	ΔV_{LDR}	I_{OUT} = 1mA to 500mA	MAX603C/E		60	100	mV
			MAX603M			150	
		I_{OUT} = 1mA to 300mA	MAX604		30	100	
Line Regulation	ΔV_{LNR}	(V_{OUT} + 0.5V) ≤ V_{IN} ≤ 11.5V, I_{OUT} = 25mA			7	40	mV
Dropout Voltage (Note 3)	ΔV_{DO}	I_{OUT} = 200mA	MAX603		130	220	mV
		I_{OUT} = 500mA			320	550	
		I_{OUT} = 200mA	MAX604		240	410	
		I_{OUT} = 400mA			480	820	
Quiescent Current	I_Q	3.0V ≤ V_{IN} ≤ 11.5V, SET = OUT	MAX60_C/E		15	35	µA
			MAX60_M			40	
OFF Quiescent Current	$I_{Q\ OFF}$	$\overline{OFF}$ ≤ 0.4V, R_L = 1kΩ, (V_{OUT} + 1V) ≤ V_{IN} ≤ 11.5V	MAX60_C		0.01	2	µA
			MAX60_E			10	
			MAX60_M			20	
Minimum Load Current	$I_{OUT\ MIN}$	V_{IN} = 11.5V, SET = OUT	MAX60_C			2	µA
			MAX60_E			6	
			MAX60_M			20	
Foldback Current Limit (Note 4)	I_{LIM}	V_{OUT} < 0.8V			350		mA
		V_{OUT} > 0.8V and V_{IN} - V_{OUT} > 0.7V			1200		
Thermal Shutdown Temperature	T_{SD}				160		°C
Thermal Shutdown Hysteresis	ΔT_{SD}				10		°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 6V (MAX603) or 4.3V (MAX604), C_{IN} = C_{OUT} = 10µF, $\overline{OFF}$ = V_{IN}, SET = GND, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reverse-Current Protection Threshold (Note 5)	ΔV_{RTH}	V_{OUT} = 4.5V	MAX603		6	20	mV
		V_{OUT} = 3.0V	MAX604		6	20	
Reverse Leakage Current	I_{RVL}	V_{IN} = 0V, V_{OUT} = 4.5V (MAX603) V_{OUT} = 3.0V (MAX604)	MAX60_C		0.01	10	µA
			MAX60_E			20	
			MAX60_M			100	
Start-Up Overshoot	V_{OSH}	R_L = 1kΩ, C_{OUT} = 10µF, $\overline{OFF}$ rise time ≤ 1µs			2		$\%V_{OUT}$
Time Required to Exit Shutdown	t_{START}	V_{IN} = 9V, R_L = 18Ω, $V_{\overline{OFF}}$ switched from 0V to V_{IN}, time from 0% to 95% of V_{OUT}			200		µs
Dual-Mode SET Threshold	$V_{SET\ TH}$	For internal feedback			80	30	mV
		For external feedback		150	80		
SET Reference Voltage	V_{SET}	SET = OUT, R_L = 1kΩ		1.16	1.20	1.24	V
SET Input Leakage Current	I_{SET}	V_{SET} = 1.5V or 0V			±0.01	±10	nA
OUT Leakage Current	$I_{OUT\ LKG}$	V_{IN} = 11.5V, V_{OUT} = 2V, SET = OUT	MAX60_C		0.01	2	µA
			MAX60_E			6	
			MAX60_M			20	
$\overline{OFF}$ Threshold Voltage	$V_{IL\ \overline{OFF}}$	Off				0.4	V
	$V_{IH\ \overline{OFF}}$	On, SET = OUT, V_{IN} = 4V		2.0			
		On, SET = OUT, V_{IN} = 6V		3.0			
		On, SET = OUT, V_{IN} = 11.5V		4.0			
$\overline{OFF}$ Input Leakage Current	$I_{\overline{OFF}}$	$V_{\overline{OFF}}$ = V_{IN} or GND			±0.01	±10	nA
Output Noise (Note 6)	e_n	10Hz to 10kHz, SET = OUT, R_L = 1kΩ, C_{OUT} = 10µF			250		μV_{RMS}

Note 1: Electrical specifications are measured by pulse testing and are guaranteed for a junction temperature (T_J) equal to the operating temperature range. C and E grade parts may be operated up to a T_J of +125°. Expect performance similar to M grade specifications. For T_J between +125°C and +150°C, the output voltage may drift more.

Note 2: (V_{IN} - V_{OUT}) is limited to keep the product (I_{OUT} x (V_{IN} - V_{OUT})) from exceeding the package power dissipation limits.

Note 3: Dropout Voltage is (V_{IN} - V_{OUT}) when V_{OUT} falls to 100mV below its nominal value at V_{IN} = V_{OUT} + 2V. For example, the MAX603 is tested by measuring the V_{OUT} at V_{IN} = 7V, then V_{IN} is lowered until V_{OUT} falls 100mV below the measured value. The difference (V_{IN} - V_{OUT}) is then measured and defined as ΔV_{DO}.

Note 4: Foldback Current Limit was characterized by pulse testing to remain below the maximum junction temperature.

Note 5: The Reverse-Current Protection Threshold is the output/input differential voltage (V_{OUT} - V_{IN}) at which reverse-current protection switchover occurs and the pass transistor is turned off.

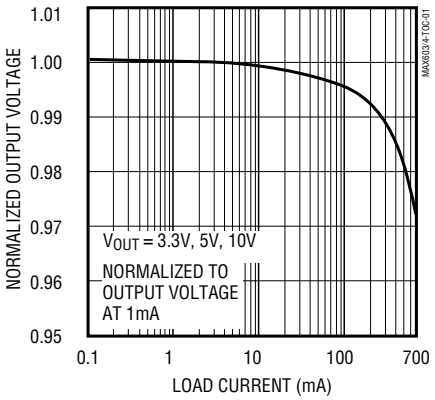
Note 6: Noise is tested using a bandpass amplifier with two poles at 10Hz and two poles at 10kHz.

5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulators

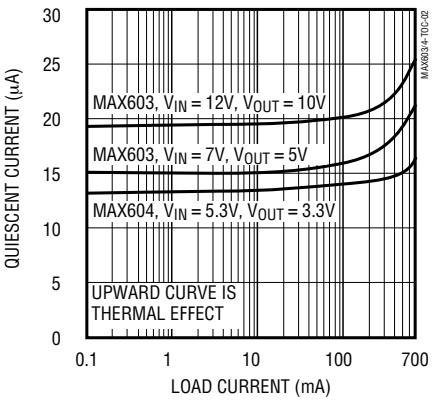
Typical Operating Characteristics

(V_{IN} = 7V for MAX603, V_{IN} = 5.3V for MAX604, $\overline{OFF}$ = V_{IN}, SET = GND, C_{IN} = C_{OUT} = 10µF, R_L = 1kΩ, T_J = +25°C, unless otherwise noted.)

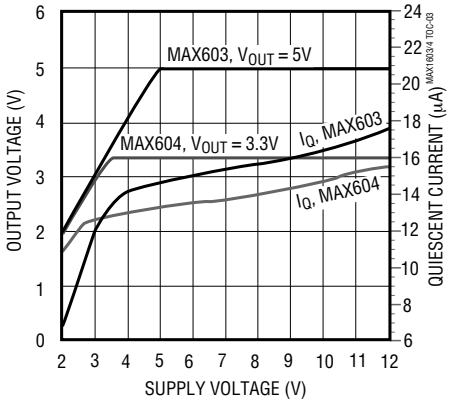
OUTPUT VOLTAGE vs. LOAD CURRENT



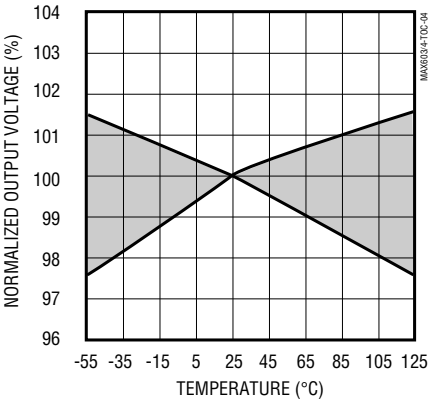
QUIESCENT CURRENT vs. LOAD CURRENT



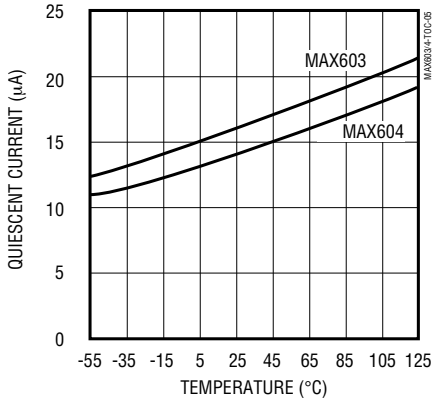
OUTPUT VOLTAGE AND QUIESCENT CURRENT vs. SUPPLY VOLTAGE



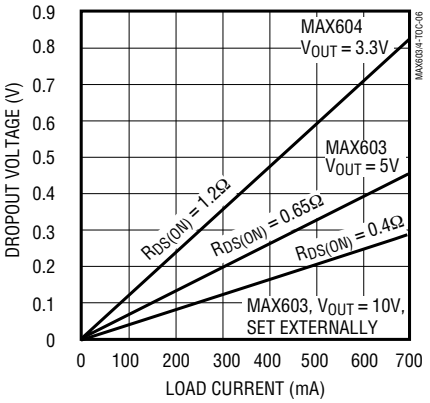
OUTPUT VOLTAGE vs. TEMPERATURE



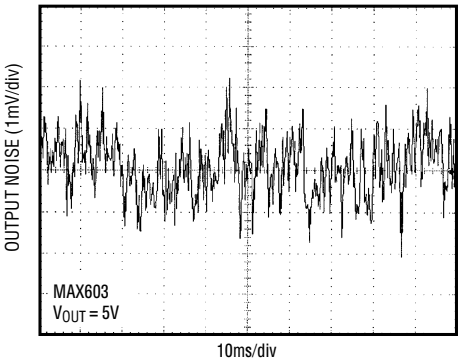
QUIESCENT CURRENT vs. TEMPERATURE



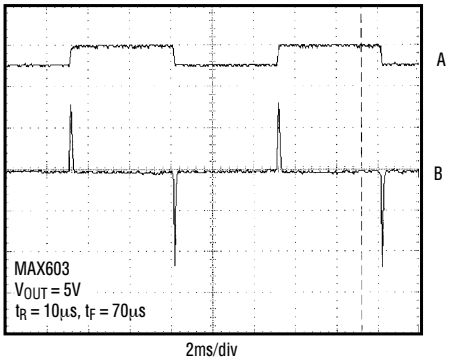
DROPOUT VOLTAGE vs. LOAD CURRENT



10Hz TO 10kHz OUTPUT NOISE



LINE-TRANSIENT RESPONSE

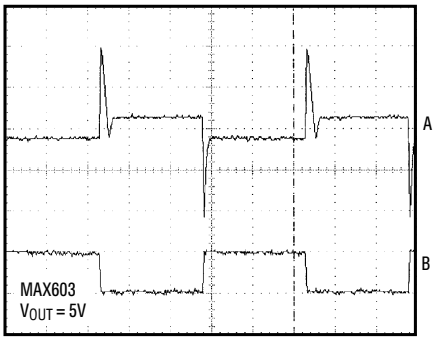


A: V_{IN} = 8V (HIGH), V_{IN} = 7V (LOW)
B: OUTPUT VOLTAGE (50mV/div)

Typical Operating Characteristics (continued)

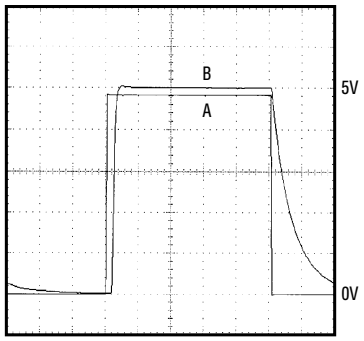
(V_{IN} = 7V for MAX603, V_{IN} = 5.3V for MAX604, $\overline{OFF}$ = V_{IN}, SET = GND, C_{IN} = C_{OUT} = 10µF, R_L = 1kΩ, T_J = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE



A: OUTPUT VOLTAGE (100mV/div)
B: I_{OUT} = 500mA (HIGH), I_{OUT} = 5mA (LOW)

OVERSHOOT AND TIME EXITING SHUTDOWN MODE



A: $\overline{OFF}$ PIN VOLTAGE (1V/div)
RISE TIME = 13µs
B: MAX603 OUTPUT VOLTAGE (1V/div)
DELAY = 4.936ms, OVERSHOOT = 1%, RISE TIME = 55µs

Pin Description

PIN	NAME	DESCRIPTION
1	IN	Regulator Input. Supply voltage can range from 2.7V to 11.5V.
2, 3, 6, 7	GND	Ground. These pins function as heatsinks, only in the SOIC package. All GND pins must be soldered to the circuit board for proper power dissipation. Connect to large copper pads or planes to channel heat from the IC.
4	$\overline{OFF}$	Shutdown, active low. Switch logic levels in less than 1µs with the high level above the $\overline{OFF}$ threshold.
5	SET	Feedback for Setting the Output Voltage. Connect to GND to set the output voltage to the preselected 3.3V or 5V. Connect to an external resistor network for adjustable output operation.
8	OUT	Regulator Output. Fixed or adjustable from 1.25V to 11.0V. Sources up to 500mA for input voltages above 4V.

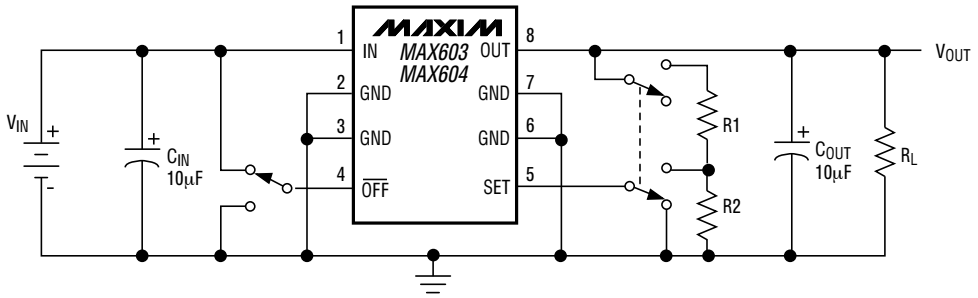


Figure 1. Test Circuit

5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulators

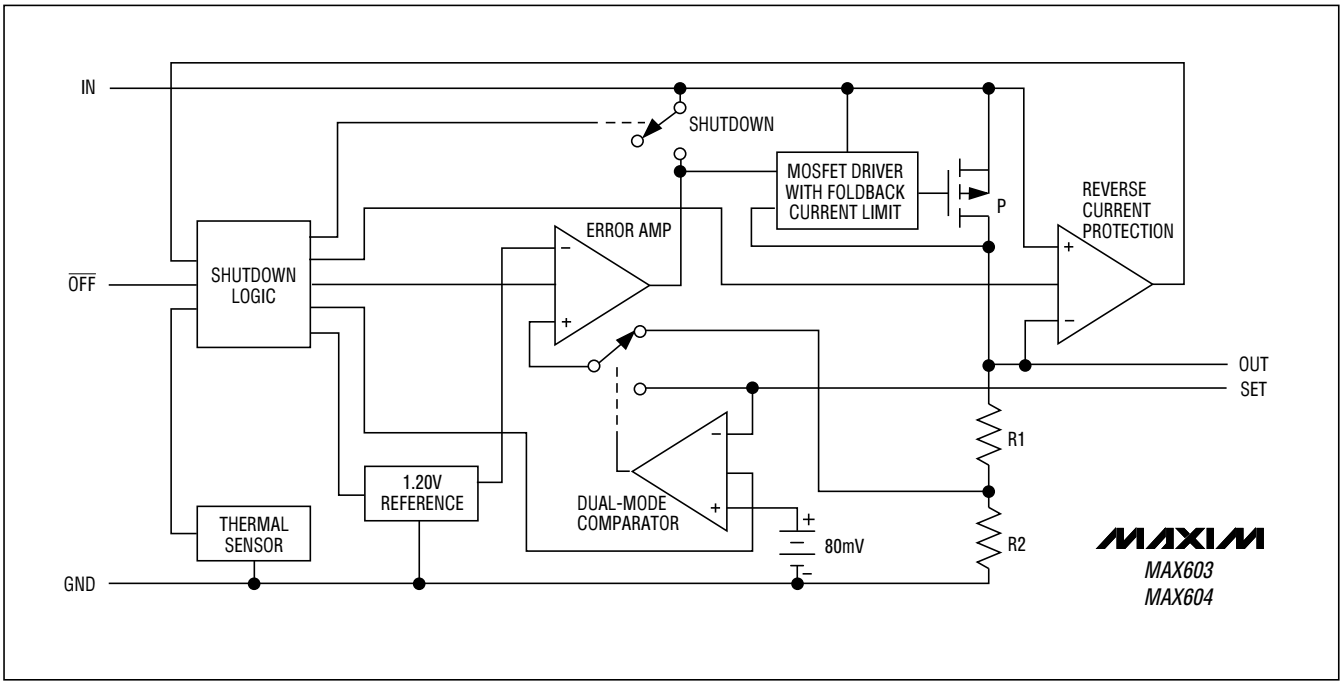


Figure 2. Functional Diagram

Detailed Description

The MAX603/MAX604 are low-dropout, low-quiescent-current linear regulators designed primarily for battery-powered applications. They supply an adjustable 1.25V to 11V output or a preselected 5V (MAX603) or 3.3V (MAX604) output for load currents up to 500mA. As illustrated in Figure 2, they consist of a 1.20V reference, error amplifier, MOSFET driver, P-channel pass transistor, dual-mode comparator, and internal feedback voltage divider.

The 1.20V bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel pass transistor. If the feedback voltage is lower than the reference, the pass transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is too high, the pass transistor gate is pulled up, allowing less current to pass to the output.

The output voltage is fed back through either an internal resistor voltage divider connected to the OUT pin, or an external resistor network connected to the SET pin. The dual-mode comparator examines the SET voltage and selects the feedback path used. If SET is below 80mV, internal feedback is used and the output voltage is regulated to 5V for the MAX603 or 3.3V for the MAX604. Additional blocks include a foldback current limiter, reverse current protection, thermal sensor, and shutdown logic.

Internal P-Channel Pass Transistor

The MAX603/MAX604 feature a 500mA P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP pass transistors, including longer battery life.

The P-channel MOSFET requires no base drive, which reduces quiescent current considerably. PNP based regulators waste considerable amounts of current in dropout when the pass transistor saturates. They also use high base-drive currents under large loads. The MAX603/MAX604 do not suffer from these problems and consume only 15µA of quiescent current under light and heavy loads, as well as in dropout.

Output Voltage Selection

The MAX603/MAX604 feature dual-mode operation. In preset voltage mode, the output of the MAX603 is set to 5V and the output of the MAX604 is set to 3.3V using internal, trimmed feedback resistors. Select this mode by connecting SET to ground.

In adjustable mode, an output between 1.25V and 11V is selected using two external resistors connected as a voltage divider to SET (Figure 3). The output voltage is set by the following equation:

$$V_{OUT} = V_{SET}\left(1 + \frac{R1}{R2}\right)$$

where V_{SET} = 1.20V. To simplify resistor selection:

$$R1 = R2\left(\frac{V_{OUT}}{V_{SET}} - 1\right)$$

Since the input bias current at SET is nominally zero, large resistance values can be used for R1 and R2 to minimize power consumption without losing accuracy. Up to 1.5MΩ is acceptable for R2. Since the V_{SET} tolerance is less than ±40mV, the output can be set using fixed resistors instead of trim pots.

In preset voltage mode, impedances between SET and ground should be less than 10kΩ. Otherwise, spurious conditions could cause the voltage at SET to exceed the 80mV dual-mode threshold.

Shutdown

A low input on the $\overline{OFF}$ pin shuts down the MAX603/MAX604. In the off mode, the pass transistor, control circuit, reference, and all biases are turned off, reducing the supply current below 2µA. $\overline{OFF}$ should be connected to IN for normal operation.

Use a fast comparator, Schmitt trigger, or CMOS or TTL logic to drive the $\overline{OFF}$ pin in and out of shutdown. Rise times should be shorter than 1µs. Do not use slow RC circuits, leave $\overline{OFF}$ open, or allow the input to linger between thresholds; these measures will prevent the output from jumping to the positive supply rail in response to an indeterminate input state.

Since the $\overline{OFF}$ threshold varies with input supply voltage (see *Electrical Characteristics*), do not derive the drive voltage from 3.3V logic. With V_{IN} at 11.5V, the high $\overline{OFF}$ logic level needs to be above 4V.

Foldback Current Limiting

The MAX603/MAX604 also include a foldback current limiter. It monitors and controls the pass transistor's gate voltage, estimating the output current and limiting it to 1.2A for output voltages above 0.8V and $V_{IN} - V_{OUT}$ > 0.7V. For $V_{IN} - V_{OUT}$ < 0.7V (dropout operation), there is no current limit. If the output voltage drops below 0.8V, implying a short-circuit condition, the output current is limited to 350mA. The output can be shorted to ground for one minute without damaging the device if the package can dissipate V_{IN} x 350mA without exceeding T_J = +150°C.

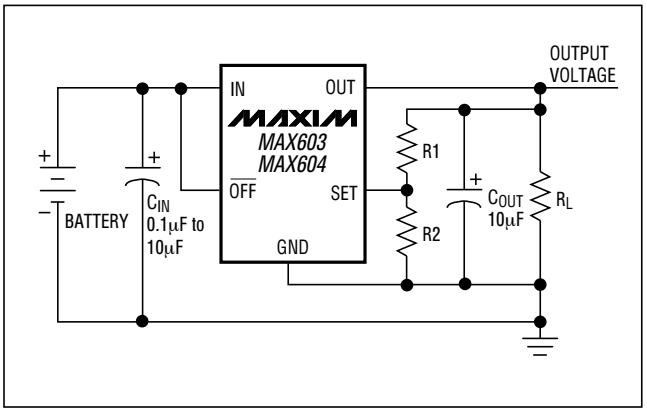


Figure 3. Adjustable Output Using External Feedback Resistors

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX603/MAX604. When the junction temperature exceeds T_J = +160°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor will turn the pass transistor on again after the IC's junction temperature cools by 10°C, resulting in a pulsed output during thermal overload conditions.

Thermal overload protection is designed to protect the MAX603/MAX604 in the event of fault conditions. For continual operation, the absolute maximum junction temperature rating of T_J = +150°C should not be exceeded.

Operating Region and Power Dissipation

Maximum power dissipation of the MAX603/MAX604 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is $P = I_{OUT}(V_{IN} - V_{OUT})$. The resulting maximum power dissipation is:

$$P_{MAX} = \left(\frac{(T_J - T_A)}{(\theta_{JB} + \theta_{BA})}\right)$$

where $(T_J - T_A)$ is the temperature difference between the MAX603/MAX604 die junction and the surrounding

5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulators

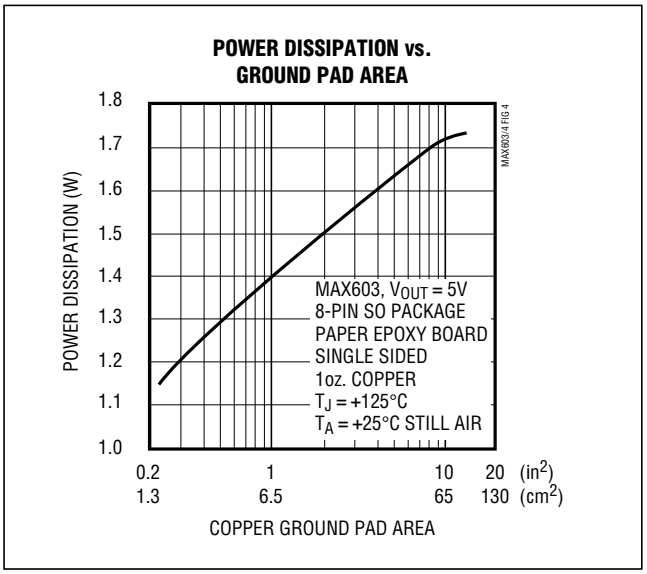


Figure 4. Typical Maximum Power Dissipation vs. Ground Pad Size.

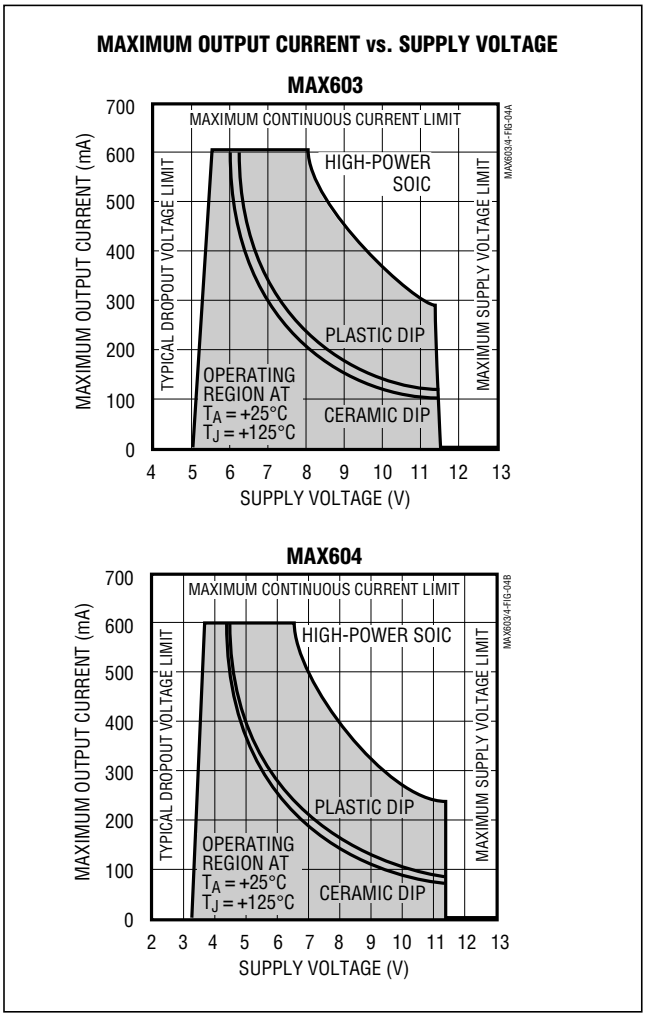


Figure 5. Power Operating Regions: Maximum Output Current vs. Differential Supply Voltage

air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package chosen, and θ_{BA} is the thermal resistance through the printed circuit board, copper traces and other materials to the surrounding air. The 8-pin SOIC package for the MAX603/MAX604 features a special lead frame with a lower thermal resistance and higher allowable power dissipation. The thermal resistance of this package is θ_{JB} = 42°C/W, compared with θ_{JB} = 110°C/W for an 8-pin plastic DIP package and θ_{JB} = 125°C/W for an 8-pin ceramic DIP package.

The GND pins of the MAX603/MAX604 SOIC package perform the dual function of providing an electrical connection to ground and channeling heat away. Connect all GND pins to ground using a large pad or ground plane. Where this is impossible, place a copper plane on an adjacent layer. The pad should exceed the dimensions in Figure 4.

Figure 4 assumes the IC is an 8-pin SOIC package, is soldered directly to the pad, has a +125°C maximum junction temperature and a +25°C ambient air temperature, and has no other heat sources. Use larger pad sizes for other packages, lower junction temperatures, higher ambient temperatures, or conditions where the IC is not soldered directly to the heat-sinking ground pad.

The MAX603/MAX604 can regulate currents up to 500mA and operate with input voltages up to 11.5V, but not simultaneously. High output currents can only be sustained when input-output differential voltages are low, as shown in Figure 5. Maximum power dissipation depends on packaging, board layout, temperature, and air flow. The maximum output current is:

$$I_{OUT(max)} = \frac{P_{MAX} \times (T_J - T_A)}{(V_{IN} - V_{OUT}) \times 100°C}$$

where P_{MAX} is derived from Figure 4.

Reverse-Current Protection

The MAX603/MAX604 has a unique protection scheme that limits reverse currents when the input voltage falls below the output. It monitors the voltages on IN and OUT and switches the IC's substrate and power bus to

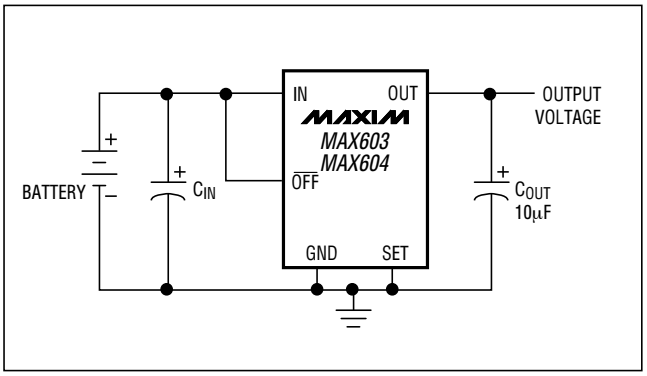


Figure 6. 3.3V or 5V Linear-Regulator Application

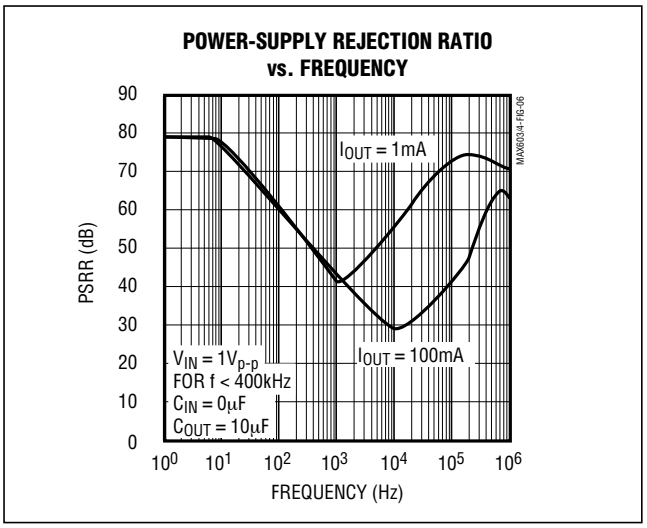


Figure 7. Power-Supply Rejection Ratio vs. Ripple Frequency

the more positive of the two. The control circuitry can then remain functioning and turn the pass transistor off, limiting reverse currents back through the device. This feature allows a backup regulator or battery pack to maintain V_{OUT} when the supply at IN fails.

Reverse-current protection activates when the voltage on IN falls 6mV (20mV maximum) below the voltage on OUT. Before this happens, currents as high as several milliamperes can flow back through the device. After switchover, typical reverse currents are limited to 0.01µA for as long as the condition exists.

Applications Information

Figure 6 illustrates the typical application for the MAX603/MAX604.

Capacitor Selection and Regulator Stability

Normally, use 0.1µF to 10µF capacitors on the input and 10µF on the output of the MAX603/MAX604. The larger input capacitor values provide better supply-noise rejection and line-transient response. Improve load-transient response, stability, and power-supply rejection by using large output capacitors. For stable operation over the full temperature range and with load currents up to 500mA, 10µF is recommended. Using capacitors smaller than 3.3µF can result in oscillation.

Noise

The MAX603/MAX604 exhibit 3mVp-p to 4mVp-p of noise during normal operation. This is negligible in most applications. When using the MAX603/MAX604 in applications that include analog-to-digital converters of greater than 12 bits, consider the ADC's power-supply rejection specifications. Refer to the output noise plot in the *Typical Operating Characteristics*.

PSRR and Operation from Sources Other than Batteries

The MAX603/MAX604 are designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. Achieving these objectives requires trading off power-supply noise rejection and swift response to supply variations and load transients. Power-supply rejection is 80dB at low freqencies and rolls off above 10Hz. As the frequency increases above 10kHz, the output capacitor is the major contributor to the rejection of power-supply noise (Figure 7). Do not use power supplies with ripple above 100kHz, especially when the ripple exceeds 100mVp-p. When operating from sources other than batteries, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output capacitors, and through passive filtering techniques. The *Typical Operating Characteristics* show the MAX603/MAX604 supply and load-transient responses.

Transient Considerations

The *Typical Operating Characteristics* show the MAX603/MAX604 load-transient response. Two components of the output response can be observed on the load-transient graphs—a DC shift from the output impedance due to the different load currents, and the transient response. Typical transients for step changes in the load current from 5mA to 500mA are 0.2V. Increasing the output capacitor's value attenuates transient spikes.

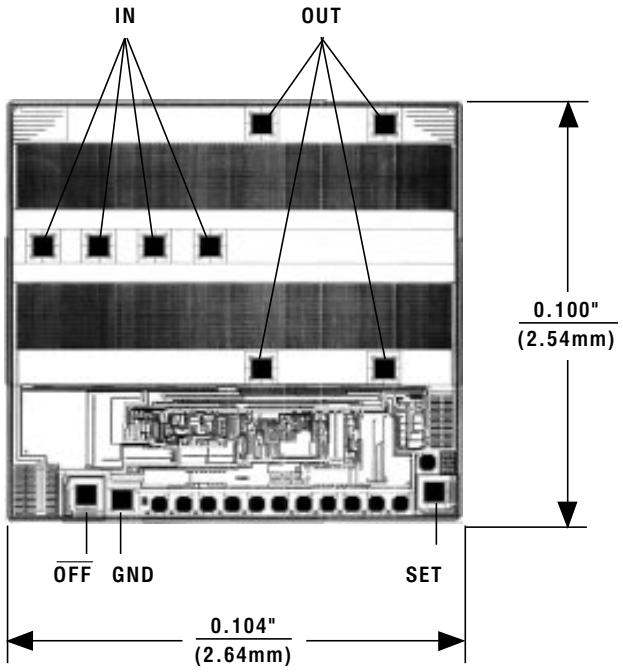
5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulators

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential, or dropout voltage, determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the MAX603/MAX604 use a P-channel MOSFET pass transistor, their dropout voltage is a function of $r_{DS(ON)}$ multiplied by the load current (see *Electrical Characteristics*).

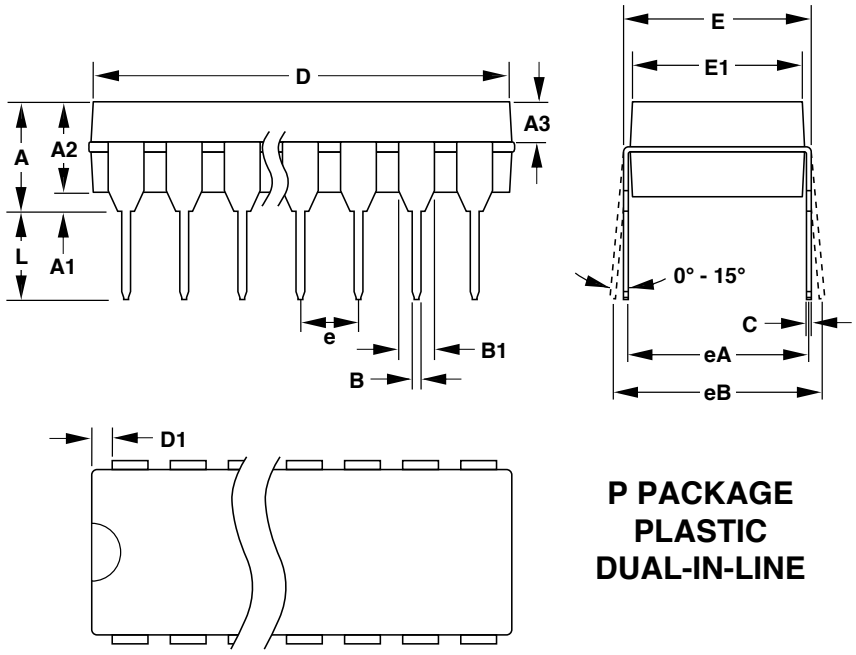
Quickly stepping up the input voltage from the dropout voltage can result in overshoot. This occurs when the pass transistor is fully on at dropout and the IC is not given time to respond to the supply voltage change. Prevent this by slowing the input voltage rise time.

Chip Topography



TRANSISTOR COUNT: 111
NO DIRECT SUBSTRATE CONNECTION. THE N-SUBSTRATE IS INTERNALLY SWITCHED BETWEEN THE MORE POSITIVE OF IN OR OUT.

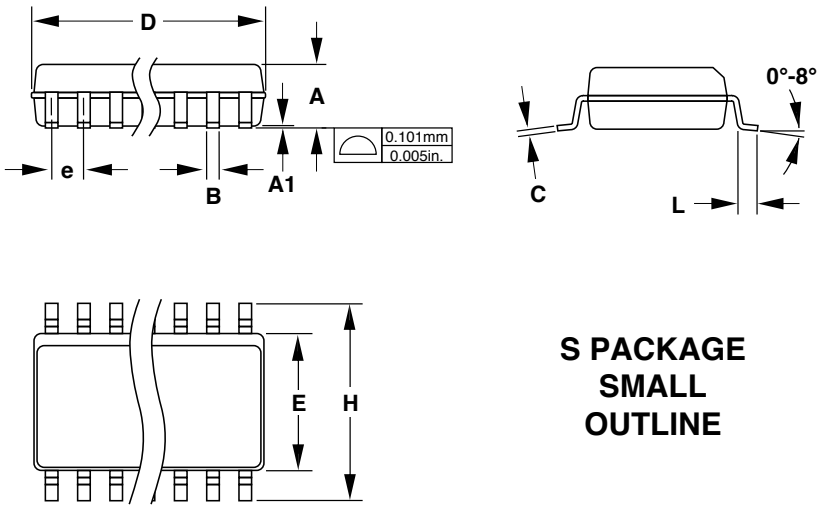
Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

P PACKAGE PLASTIC DUAL-IN-LINE

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.348	0.390	8.84	9.91
D	14	0.735	0.765	18.67	19.43
D	16	0.745	0.765	18.92	19.43
D	18	0.885	0.915	22.48	23.24
D	20	1.015	1.045	25.78	26.54
D	24	1.14	1.265	28.96	32.13



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

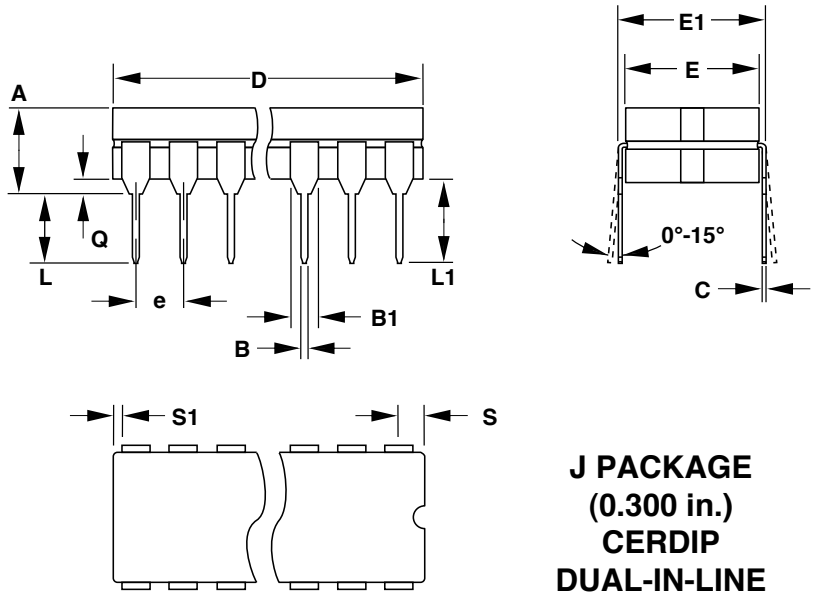
S PACKAGE SMALL OUTLINE

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A

5V/3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulators

Package Information (continued)



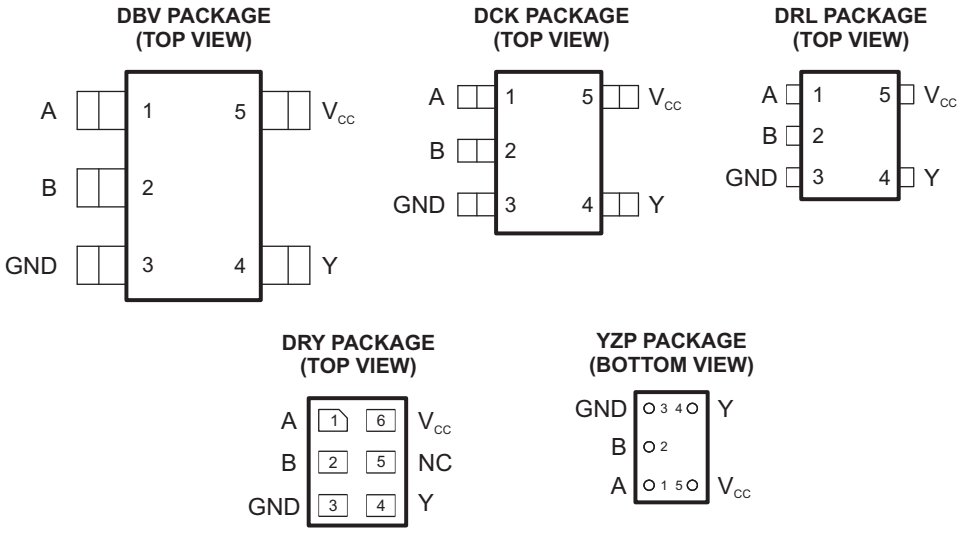
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

J PACKAGE (0.300 in.) CERDIP DUAL-IN-LINE

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

FEATURES

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Supports 5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 3.6 ns at 3.3 V**
- **Low Power Consumption, 10-μA Max I_{CC}**
- **± 24-mA Output Drive at 3.3 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**



NC – No internal connection

See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single 2-input positive-OR gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G32 performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \bullet \overline{B}}$ in positive logic.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

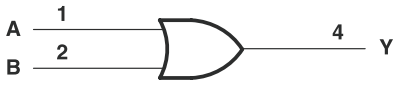
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G32YZPR	_ _ _CG_
	SON – DRY	Reel of 5000	SN74LVC1G32DRYR	CG_
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G32DBVR	C32_
			SN74LVC1G32DBVRE4	
			SN74LVC1G32DBVRG4	
		Tube of 250	SN74LVC1G32DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74LVC1G32DCKR	CG_
			SN74LVC1G32DCKRE4	
			SN74LVC1G32DCKRG4	
		Tube of 250	SN74LVC1G32DCKT	
			SN74LVC1G32DCKTE4	
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G32DRLR	CG_
			SN74LVC1G32DRLRG4	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK/DRL/DRY: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous ouput current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DBV package		206	°C/W
		DCK package		252	
		DRL package		142	
		DRY package		234	
		YZP package		132	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 μA	1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA	1.65 V	1.2			
		I_{OH} = –8 mA	2.3 V	1.9			
		I_{OH} = –16 mA	3 V	2.4			
		I_{OH} = –24 mA		2.3			
		I_{OH} = –32 mA	4.5 V	3.8			
V_{OL}		I_{OL} = 100 μA	1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 8 mA	2.3 V			0.3	
		I_{OL} = 16 mA	3 V			0.4	
		I_{OL} = 24 mA				0.55	
		I_{OL} = 32 mA	4.5 V			0.55	
I_I	A or B inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5	μA
I_{off}		V_I or V_O = 5.5 V	0			±10	μA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10	μA
ΔI_{CC}		One input at V_{CC}– 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500	μA
C_i		V_I = V_{CC} or GND	3.3 V		4		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	1.9	7.2	0.8	4.4	0.9	3.6	0.8	3.4	ns

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF or 50 pF (unless otherwise noted) (see Figure 2)

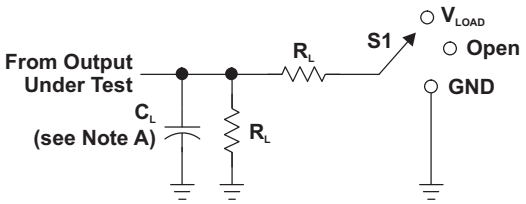
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2.8	8	1.2	5.5	1.1	4.5	1	4	ns

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	20	20	21	22	pF

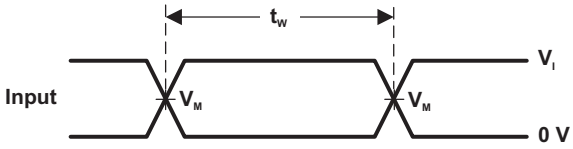
PARAMETER MEASUREMENT INFORMATION



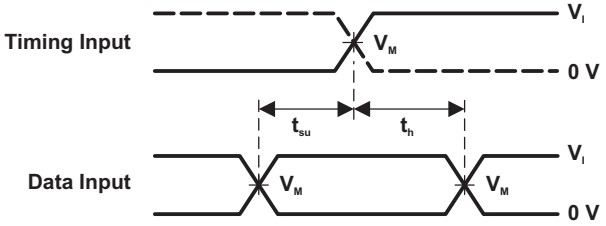
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

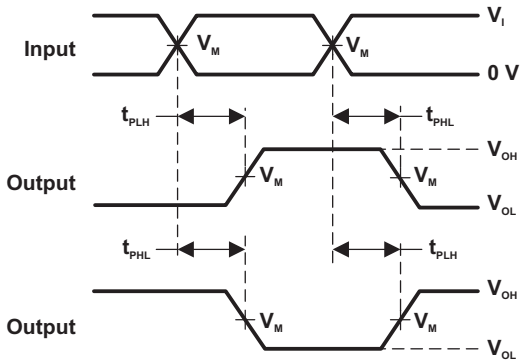
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



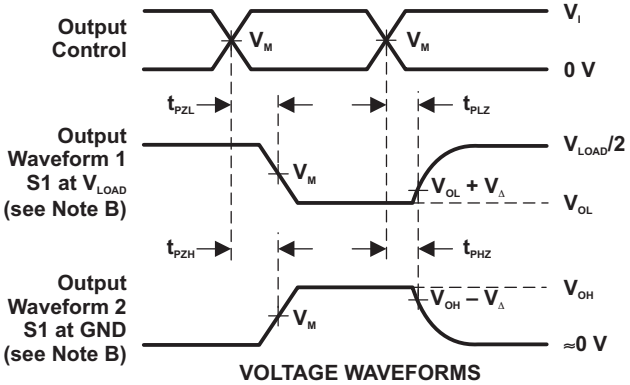
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

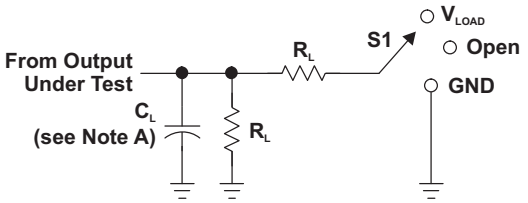


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

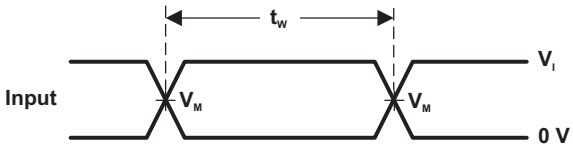
PARAMETER MEASUREMENT INFORMATION (continued)



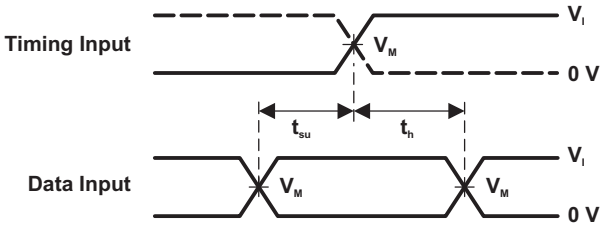
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

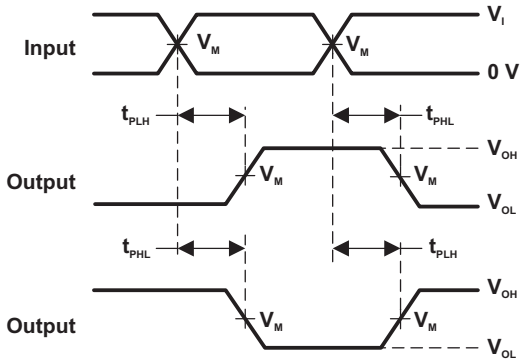
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



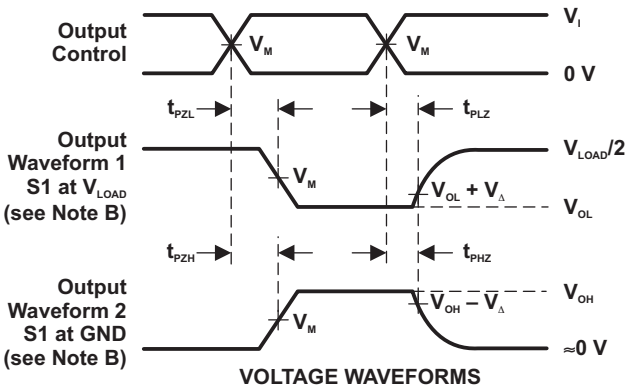
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LVC1G32DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G32YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

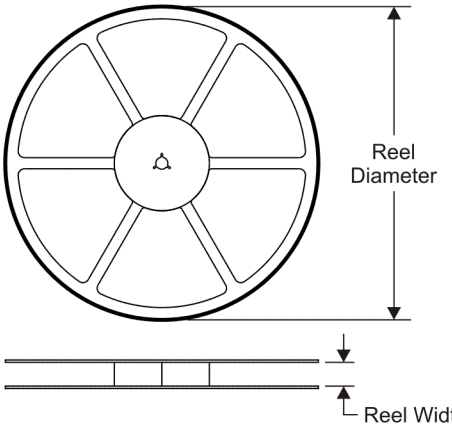
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G32 :
- Automotive: SN74LVC1G32-Q1
- Enhanced Product: SN74LVC1G32-EP

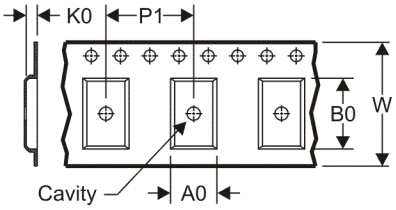
NOTE: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

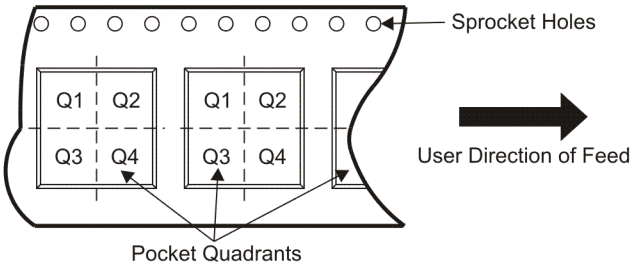


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

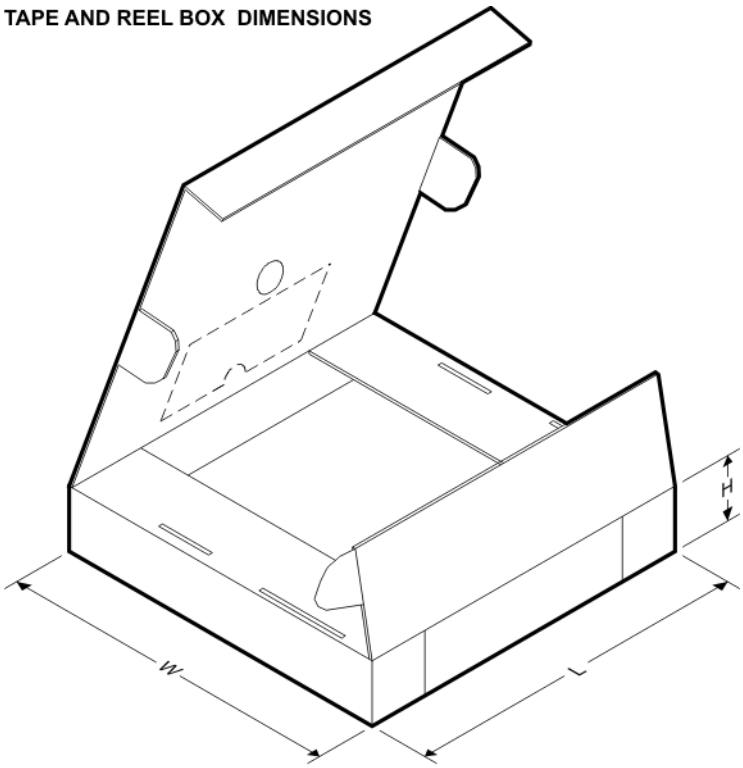
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G32DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G32DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G32DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G32DBVT	SOT-23	DBV	5	250	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G32DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G32DCKR	SC70	DCK	5	3000	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74LVC1G32DCKT	SC70	DCK	5	250	180.0	9.2	2.24	2.34	1.22	4.0	8.0	Q3
SN74LVC1G32DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G32DRLR	SOT	DRL	5	4000	180.0	9.2	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G32DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G32YZPR	DSBGA	YZP	5	3000	180.0	8.4	1.02	1.52	0.63	4.0	8.0	Q1

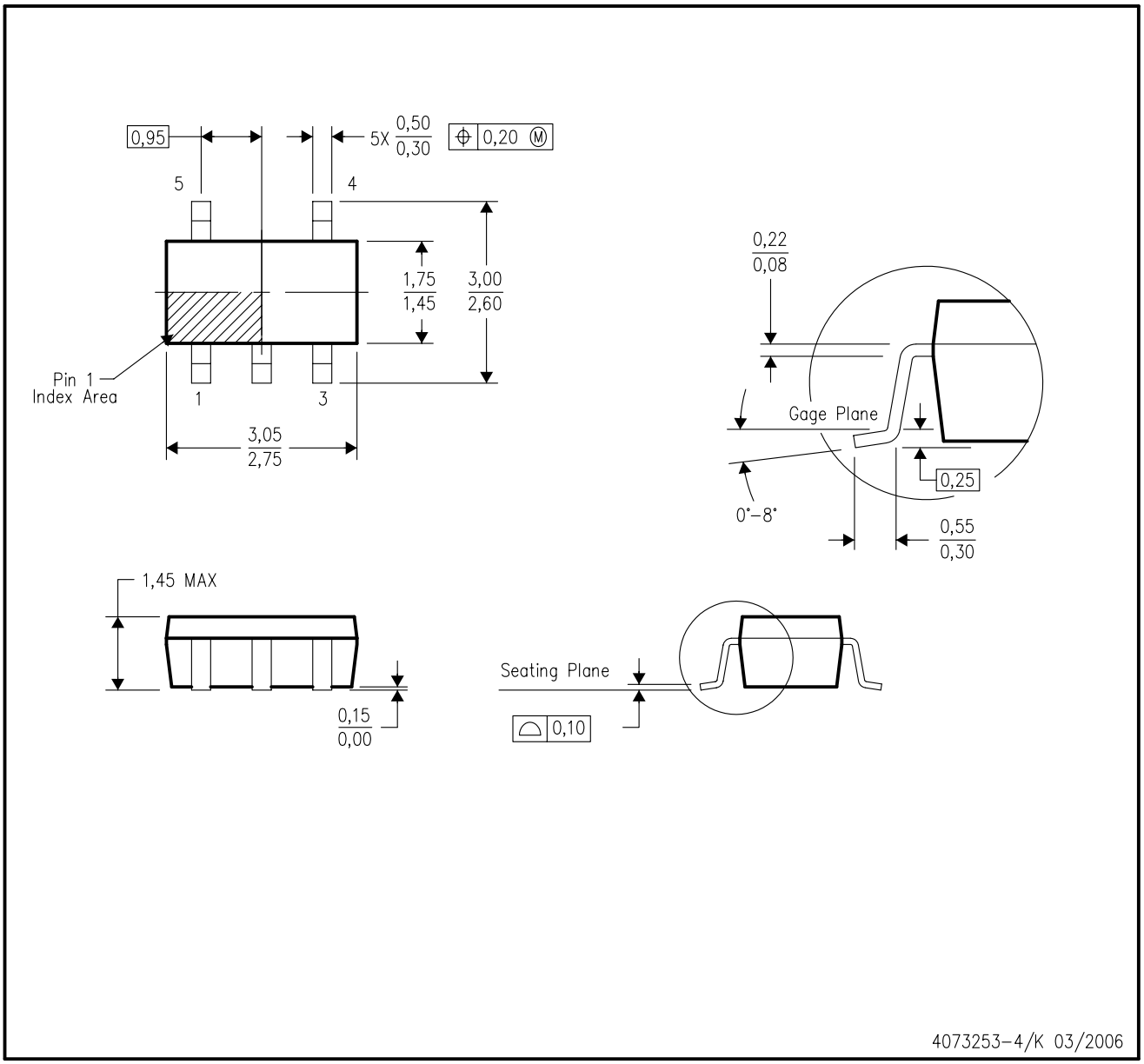
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

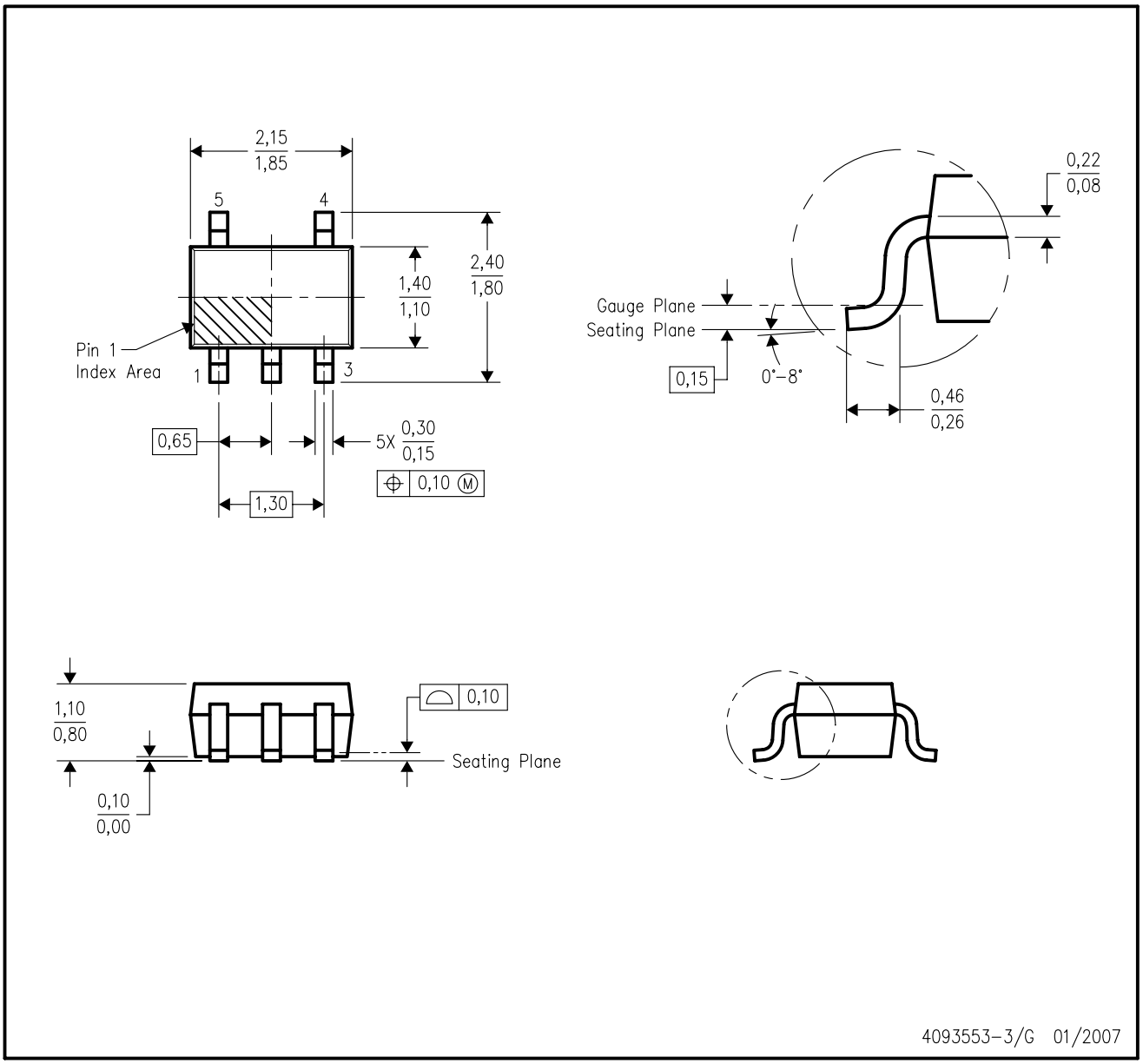
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G32DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G32DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74LVC1G32DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G32DBVT	SOT-23	DBV	5	250	205.0	200.0	33.0
SN74LVC1G32DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G32DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G32DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G32DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G32DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G32DRYR	SON	DRY	6	5000	220.0	205.0	50.0
SN74LVC1G32YZPR	DSBGA	YZP	5	3000	220.0	220.0	34.0

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

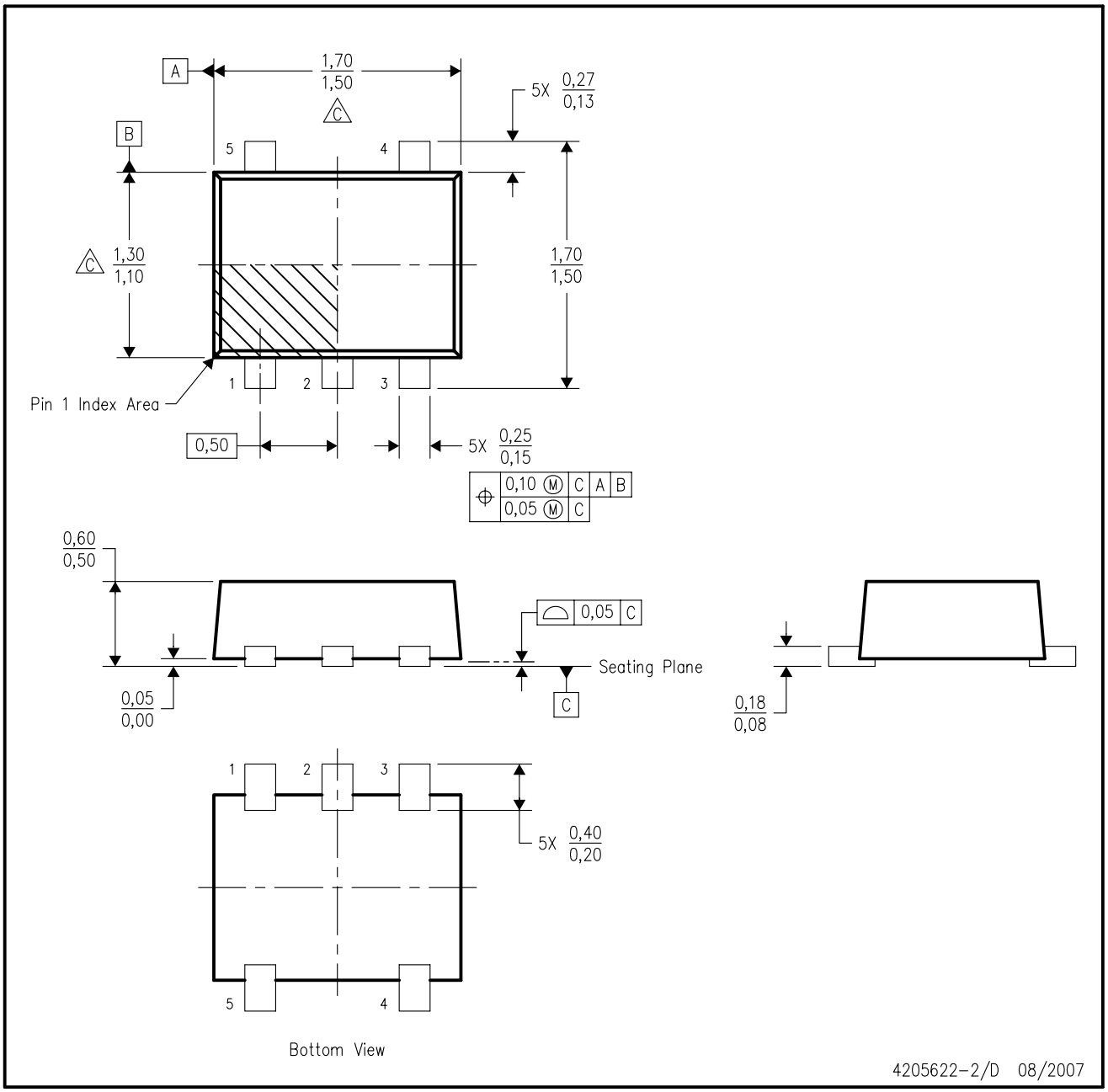


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE

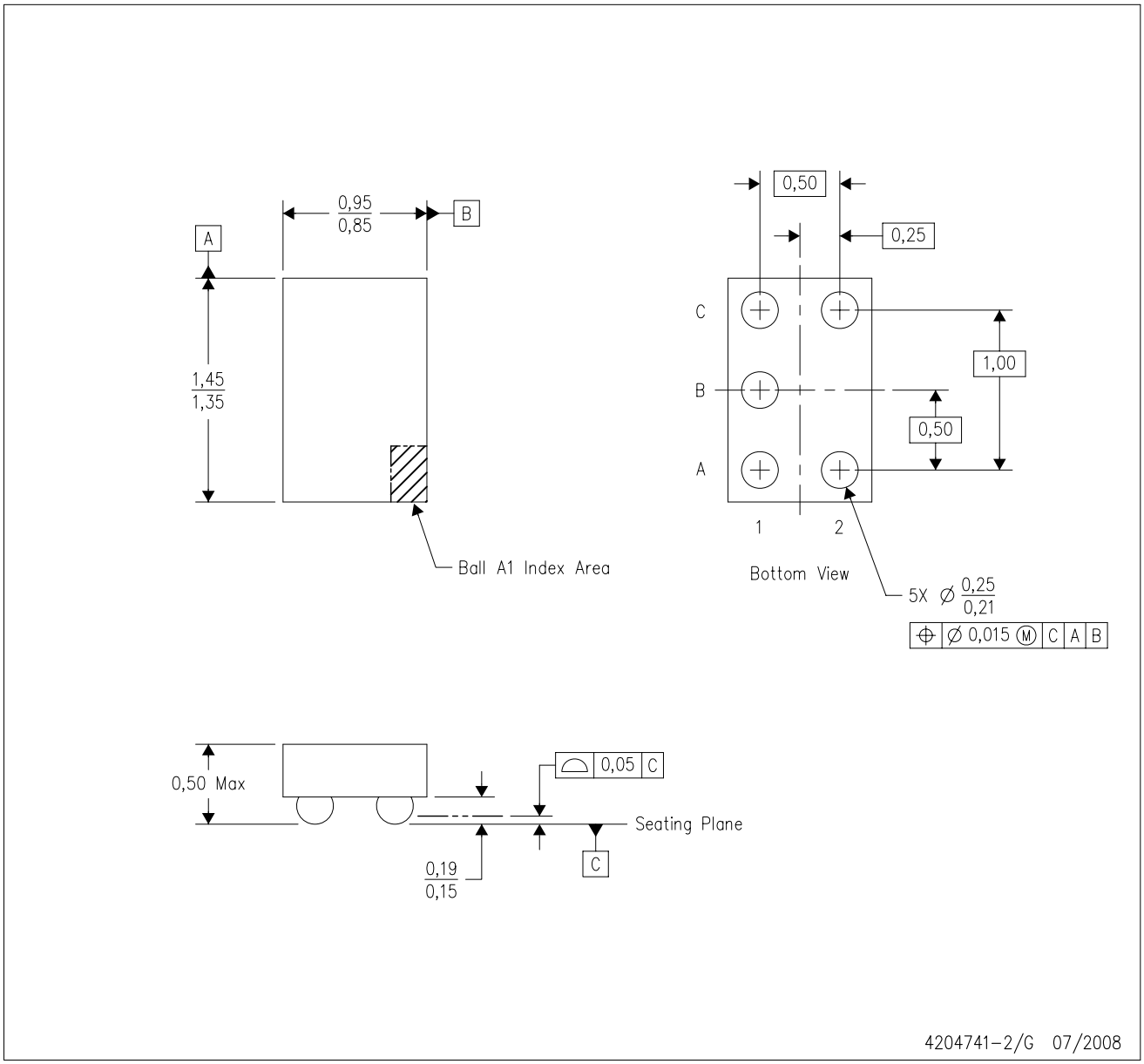


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

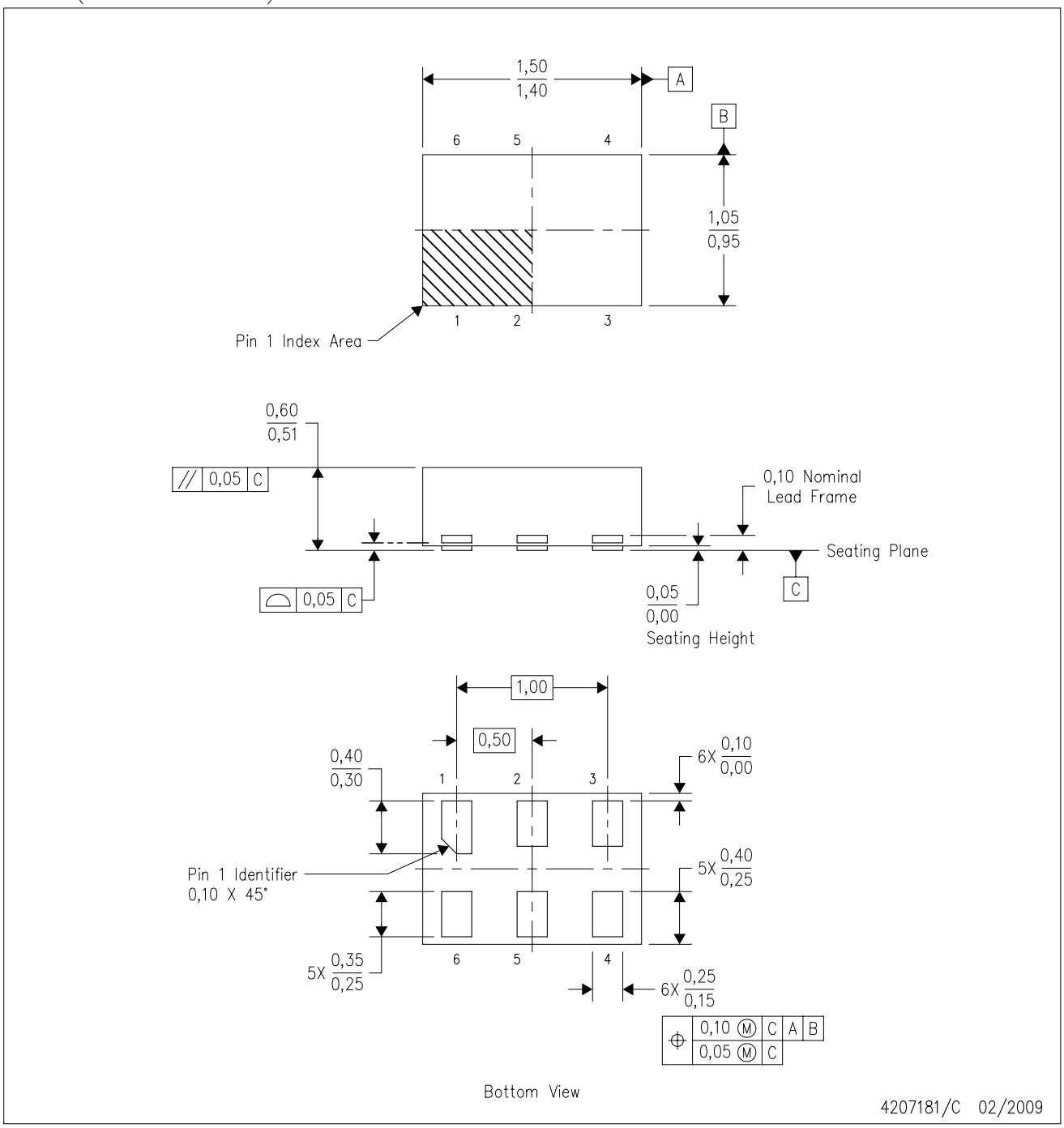
YZP (R-XBGA-N5) DIE-SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead-free. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

DRY (R–PDSO–N6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. This package complies to JEDEC MO–287 variation UFAD.

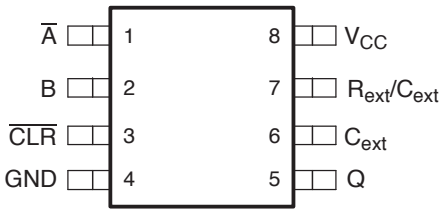
SN74LVC1G123
SINGLE RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH SCHMITT-TRIGGER INPUTS

SCES586B–JULY 2004–REVISED JANUARY 2007

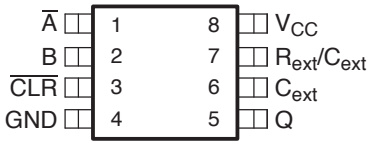
FEATURES

- **Available in the Texas Instruments NanoFree™ Package**
- **Supports 5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 8 ns at 3.3 V**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **Schmitt-Trigger Circuitry on $\overline{A}$ and B Inputs for Slow Input Transition Rates**
- **Edge Triggered From Active-High or Active-Low Gated Logic Inputs**
- **Retriggerable for Very Long Output Pulses, up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Glitch-Free Power-Up Reset on Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

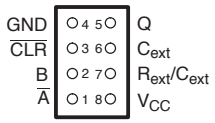
DCT PACKAGE (TOP VIEW)



DCU PACKAGE (TOP VIEW)



YZP PACKAGE (BOTTOM VIEW)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The SN74LVC1G123 is a single retriggerable monostable multivibrator designed for 1.65-V to 5.5-V V_{CC} operation.

This monostable multivibrator features output pulse-duration control by three methods. In the first method, the $\overline{A}$ input is low, and the B input goes high. In the second method, the B input is high, and the $\overline{A}$ input goes low. In the third method, the $\overline{A}$ input is low, the B input is high, and the clear ($\overline{CLR}$) input goes high.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G123YZPR	_ _ _ D8_
	SSOP – DCT	Reel of 3000	SN74LVC1G123DCTR	C23_
		Reel of 250	SN74LVC1G123DCTT	
	VSSOP – DCU	Reel of 3000	SN74LVC1G123DCUR	C23_
		Reel of 250	SN74LVC1G123DCUT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The output pulse duration is programmed by selecting external resistance and capacitance values. The external timing capacitor must be connected between C_{ext} and R_{ext}/C_{ext} (positive) and an external resistor connected between R_{ext}/C_{ext} and V_{CC}. To obtain variable pulse durations, connect an external variable resistance between R_{ext}/C_{ext} and V_{CC}. The output pulse duration also can be reduced by taking $\overline{CLR}$ low.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. The $\overline{A}$ and B inputs have Schmitt triggers with sufficient hysteresis to handle slow input transition rates with jitter-free triggering at the outputs.

Once triggered, the basic pulse duration can be extended by retriggering the gated low-level-active ($\overline{A}$) or high-level-active (B) input. Pulse duration can be reduced by taking $\overline{CLR}$ low. $\overline{CLR}$ can be used to override $\overline{A}$ or B inputs. The input/output timing diagram illustrates pulse control by retriggering the inputs and early clearing.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

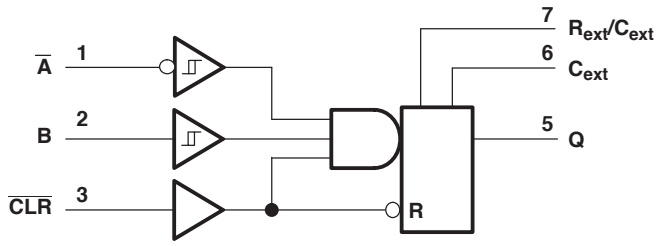
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

FUNCTION TABLE

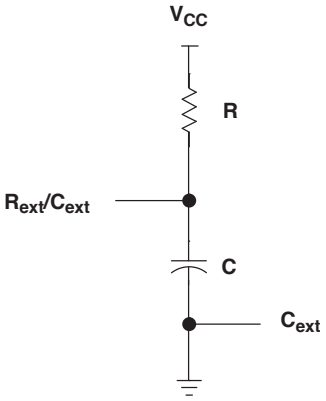
INPUTS			OUTPUTS
$\overline{CLR}$	$\overline{A}$	B	Q
L	X	X	L
X	H	X	L(1)
X	X	L	L(1)
H	L	↑	⎍
H	↓	H	⎍
↑	L	H	⎍

(1) These outputs are based on the assumption that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.

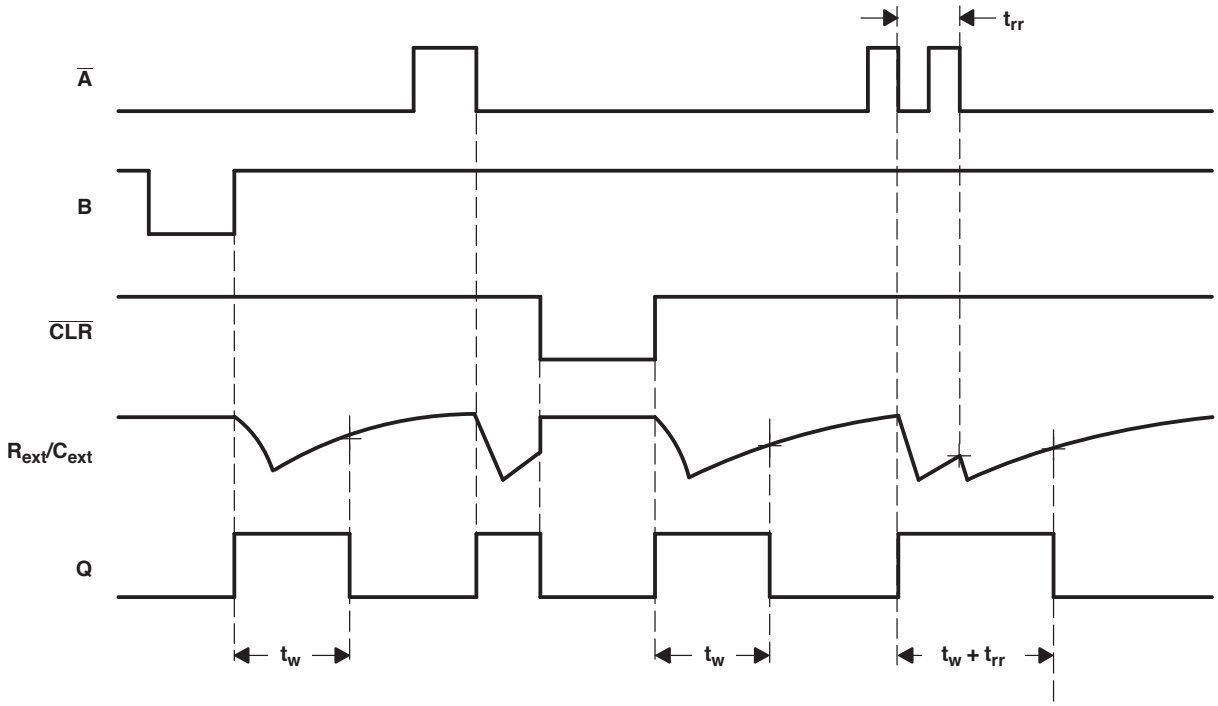
LOGIC DIAGRAM (POSITIVE LOGIC)



REQUIRED TIMING CIRCUIT



INPUT/OUTPUT TIMING DIAGRAM



Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DCT package		220	°C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 3 V		–16	
				–24	
		V_{CC} = 4.5 V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
R_{ext}(2)	External timing resistance	V_{CC} = 2 V	5 k		Ω
		V_{CC} ≥ 3 V	1 k		
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) R_{ext}/C_{ext} is an I/O and must not be connected directly to GND or V_{CC}.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		1.65 V to 5.5 V	V_{CC} – 0.1			V
		I_{OH} = –4 mA		1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	1.9			
		I_{OH} = –16 mA		3 V	2.4			
		I_{OH} = –24 mA			2.3			
		I_{OH} = –32 mA		4.5 V	3.8			
V_{OL}		I_{OL} = 100 μA		1.65 V to 5.5 V			0.1	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.3	
		I_{OL} = 16 mA		3 V			0.4	
		I_{OL} = 24 mA					0.55	
		I_{OL} = 32 mA		4.5 V			0.55	
I_I	R_{ext}/C_{ext}(2)	B = GND,	$\overline{A} = \overline{CLR} = V_{CC}$	1.65 V to 5.5 V			±0.25	μA
	$\overline{A}$, B, $\overline{CLR}$	V_I = 5.5 V or GND					±1	
I_{off}	$\overline{A}$, B, Q, $\overline{CLR}$	V_I or V_O = 5.5 V		0			±10	μA
I_{CC}	Quiescent	$V_I = V_{CC}$ or GND,	I_O = 0	5.5 V			20	μA
I_{CC}	Active state	$V_I = V_{CC}$ or GND,	R_{ext}/C_{ext} = 0.5 V_{CC}	1.65 V			165	μA
				2.3 V			220	
				3 V			280	
				4.5 V			650	
				5.5 V			975	
C_I		$V_I = V_{CC}$ or GND		3.3 V		3		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This test is performed with the terminal in the off-state condition.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			TEST CONDITIONS		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
					MIN	TYP	MIN	TYP	MIN	TYP	MIN	TYP	
t_wIN	Pulse duration	$\overline{CLR}$			8		4		3		2.5		ns
		$\overline{A}$ or B trigger			8		4		3		2.5		
t_{rr}	Pulse retrigger time		R_{ext} = 1 kΩ	C_{ext} = 100 pF						5.5		4.5	ns
				C_{ext} = 100 μF						1.4		1.1	μs
			R_{ext} = 5 kΩ	C_{ext} = 100 pF		75		45					ns
				C_{ext} = 100 μF		1.8		1.4					μs

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q	7	18.5	52	4	17	3	11.5	2	7.6	ns
	$\overline{CLR}$		5	12.4	34	3	11.5	2	8	1.5	5.5	
	$\overline{CLR}$ trigger		7	17.4	54	4	15.5	3	10.5	2	7	

Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	TYP(1)	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	$\overline{A}$ or B	Q		6	18.6	57	3	18.5	2	12.5	1.5	8.2	ns
	$\overline{CLR}$			4	11.6	36.5	2	12.5	1.5	8.6	1.5	6	
	$\overline{CLR}$ trigger			5	17.3	59	2.5	17	2	11.5	1.5	7.5	
t_wOUT(2)		Q	C_{ext} = 28 pF, R_{ext} = 2 kΩ		225	600	190	220	170	200	150	180	ns
			C_{ext} = 0.01 μF, R_{ext} = 10 kΩ		100	110	100	110	100	110	100	110	μs
			C_{ext} = 0.1 μF, R_{ext} = 10 kΩ		1	1.1	1	1.1	1	1.1	1	1.1	ms

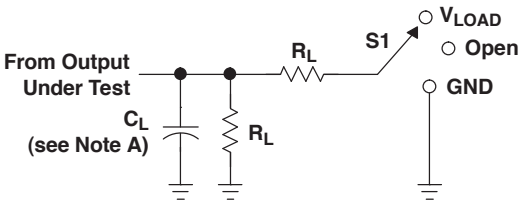
(1) T_A = 25°C
(2) t_w = Duration of pulse at Q output

Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
				TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$\overline{A}$ = low, B = high, $\overline{CLR}$ = 10 MHz	R_{ext} = 1 kΩ, No C_{ext}			35	37	pF
			R_{ext} = 5 kΩ, No C_{ext}	41	40			

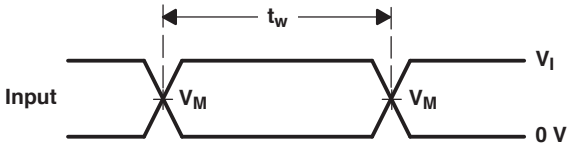
PARAMETER MEASUREMENT INFORMATION



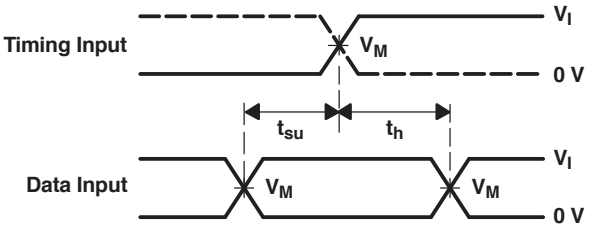
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

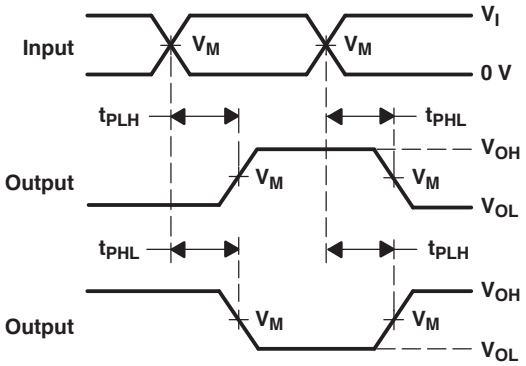
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 MΩ	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MΩ	0.3 V



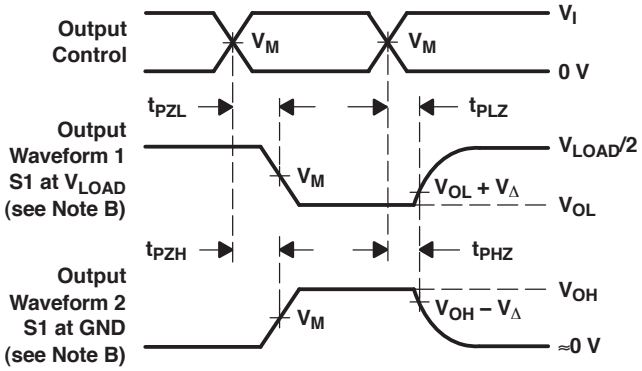
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

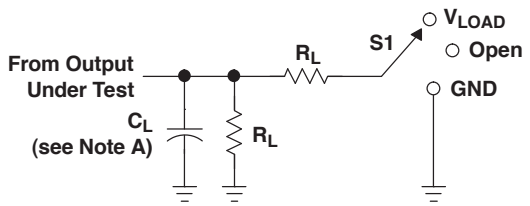


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

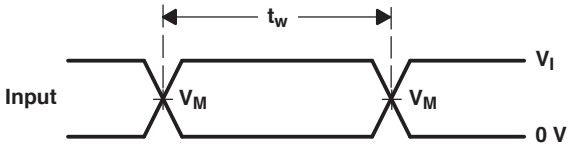
PARAMETER MEASUREMENT INFORMATION



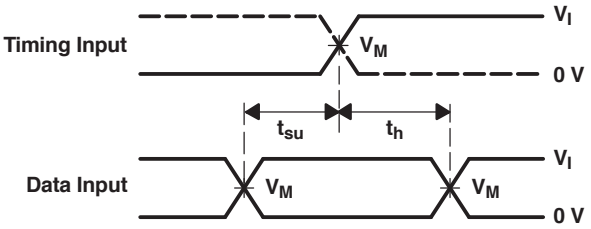
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

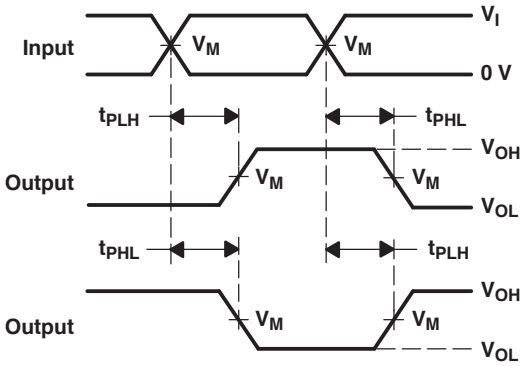
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



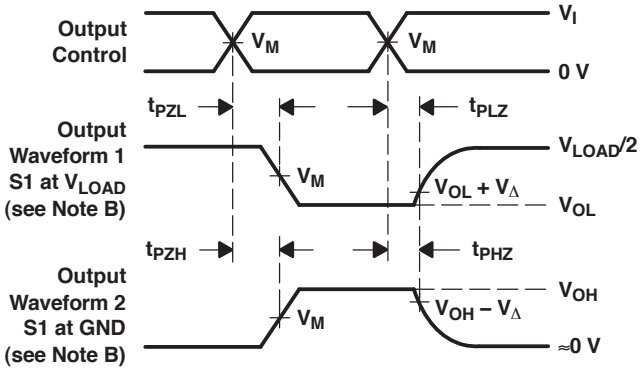
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION(1)

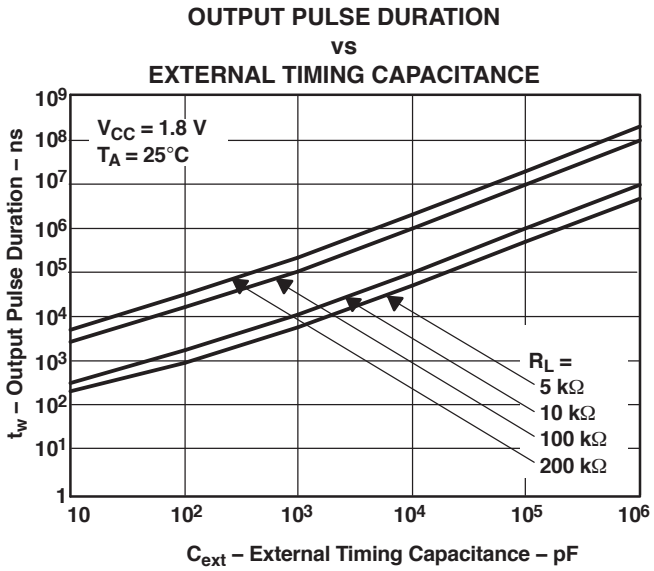


Figure 3.

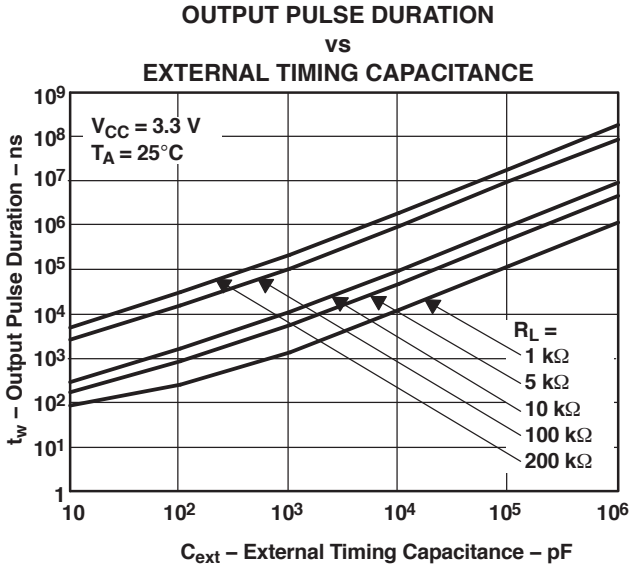


Figure 4.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

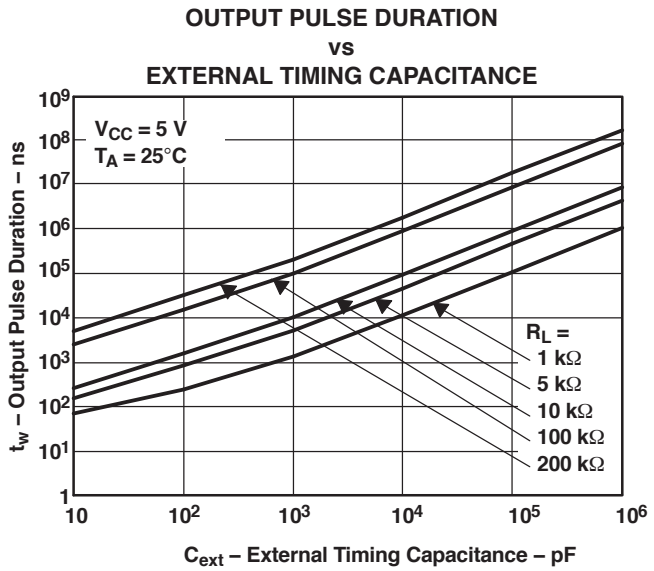


Figure 5.

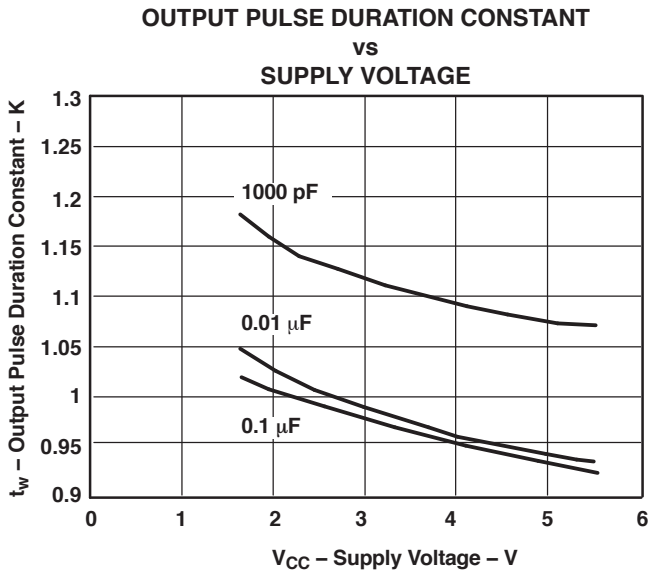


Figure 6.

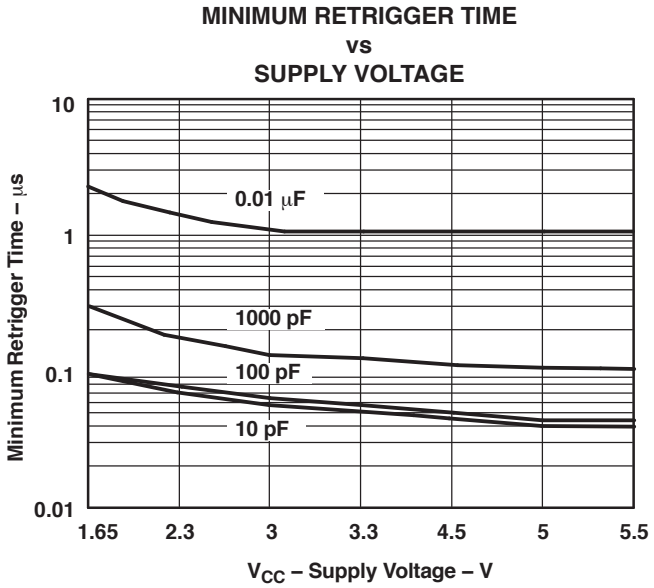

MINIMUM RETRIGGER TIME
vs
SUPPLY VOLTAGE
Minimum Retrigger Time – µs
10
1
0.1
0.01
0.01 µF
1000 pF
100 pF
10 pF
1.65
2.3
3
3.3
4.5
5
5.5
VCC – Supply Voltage – V

Figure 7.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74LVC1G123DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCTTE4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCTTG4	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC1G123DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCTT	ACTIVE	SM8	DCT	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G123YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

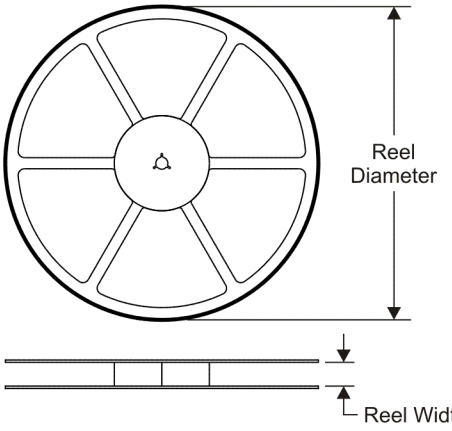
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

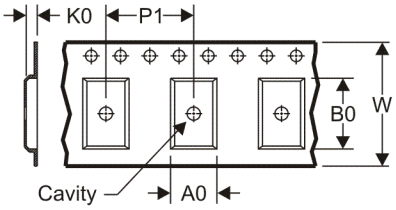
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

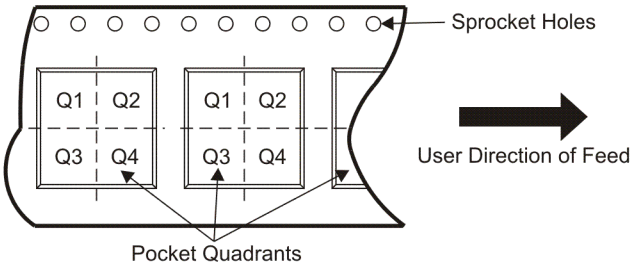


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

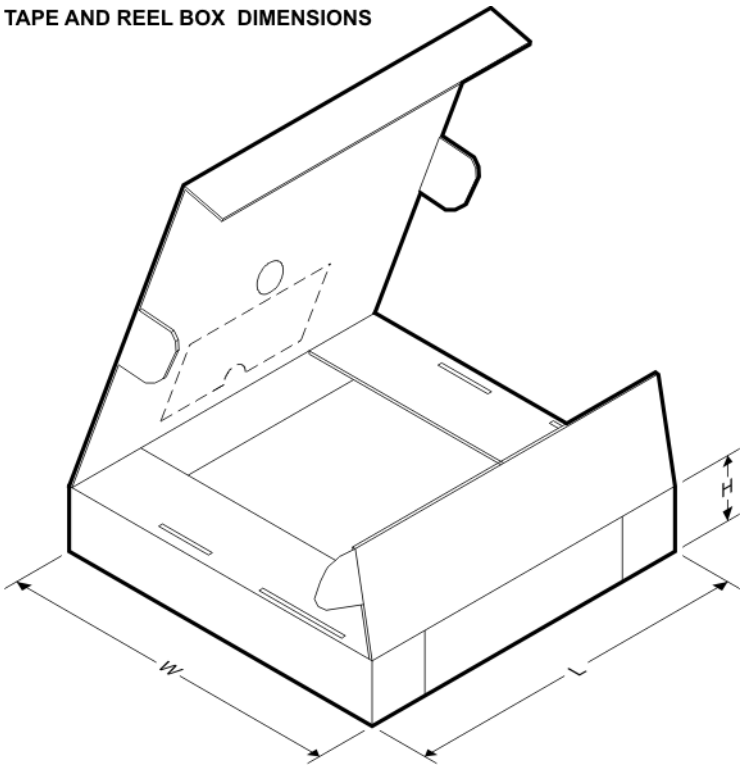
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G123DCUR	US8	DCU	8	3000	180.0	9.2	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G123YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

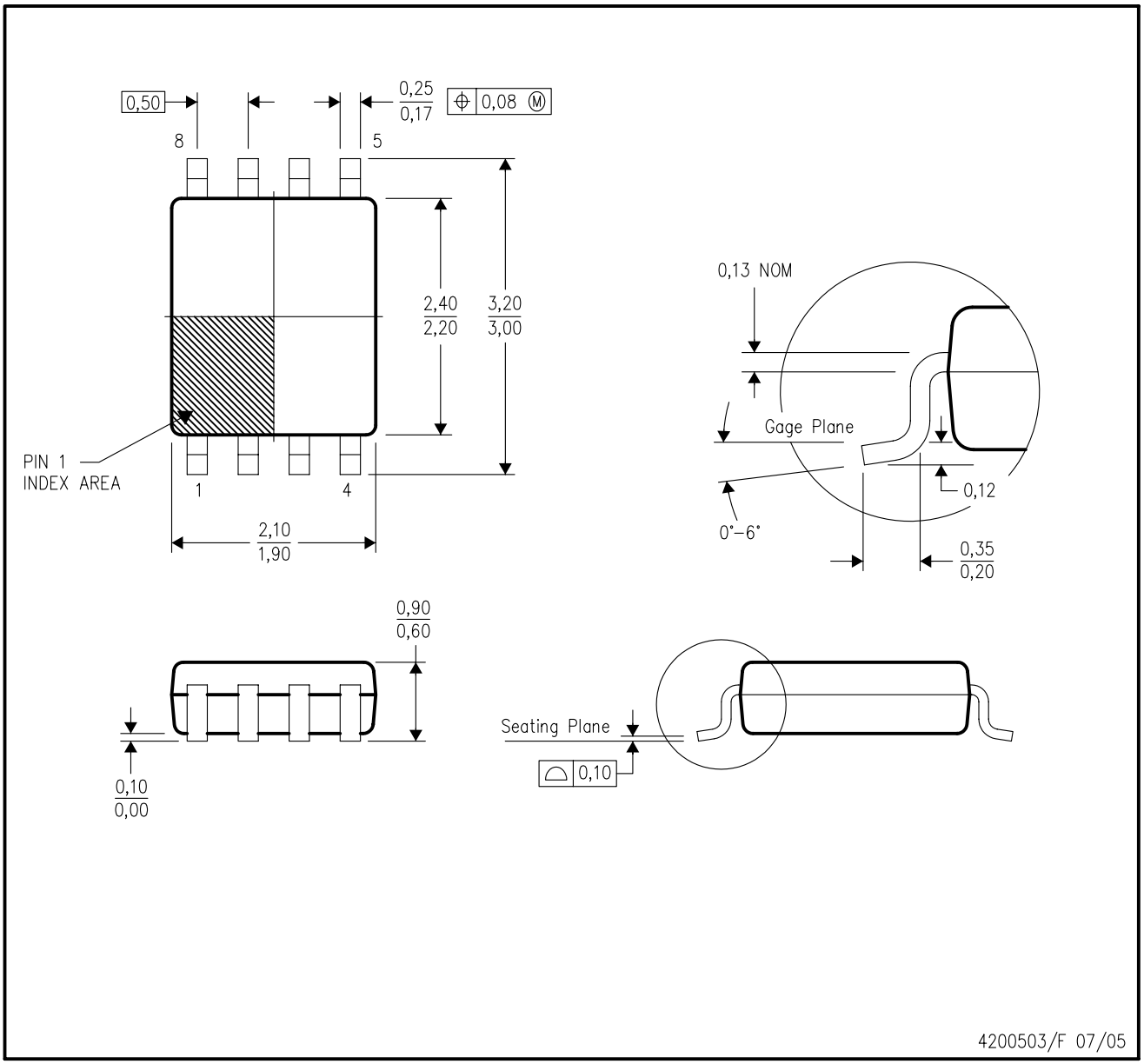
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

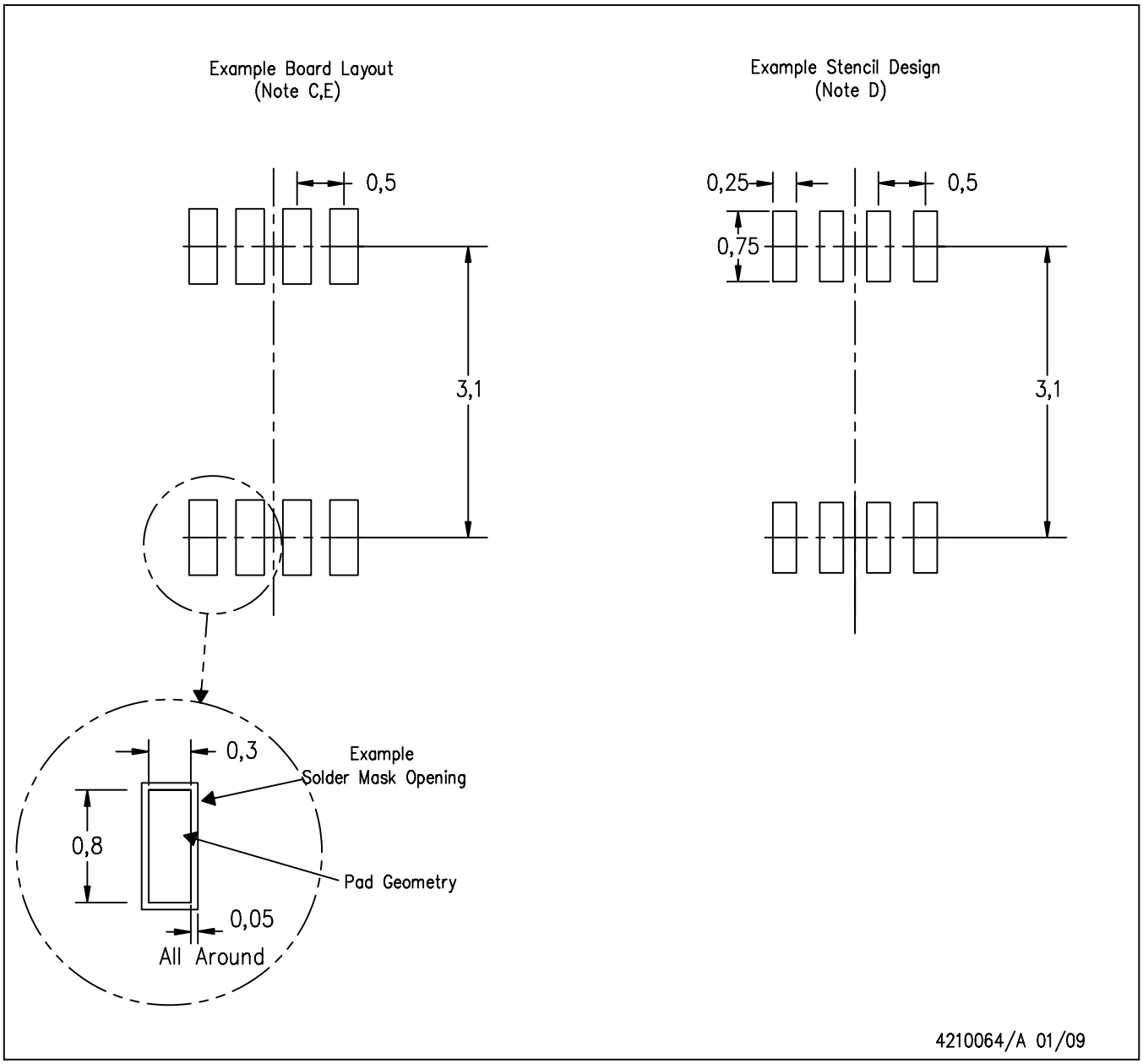
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G123DCUR	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC1G123YZPR	DSBGA	YZP	8	3000	220.0	220.0	34.0

DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



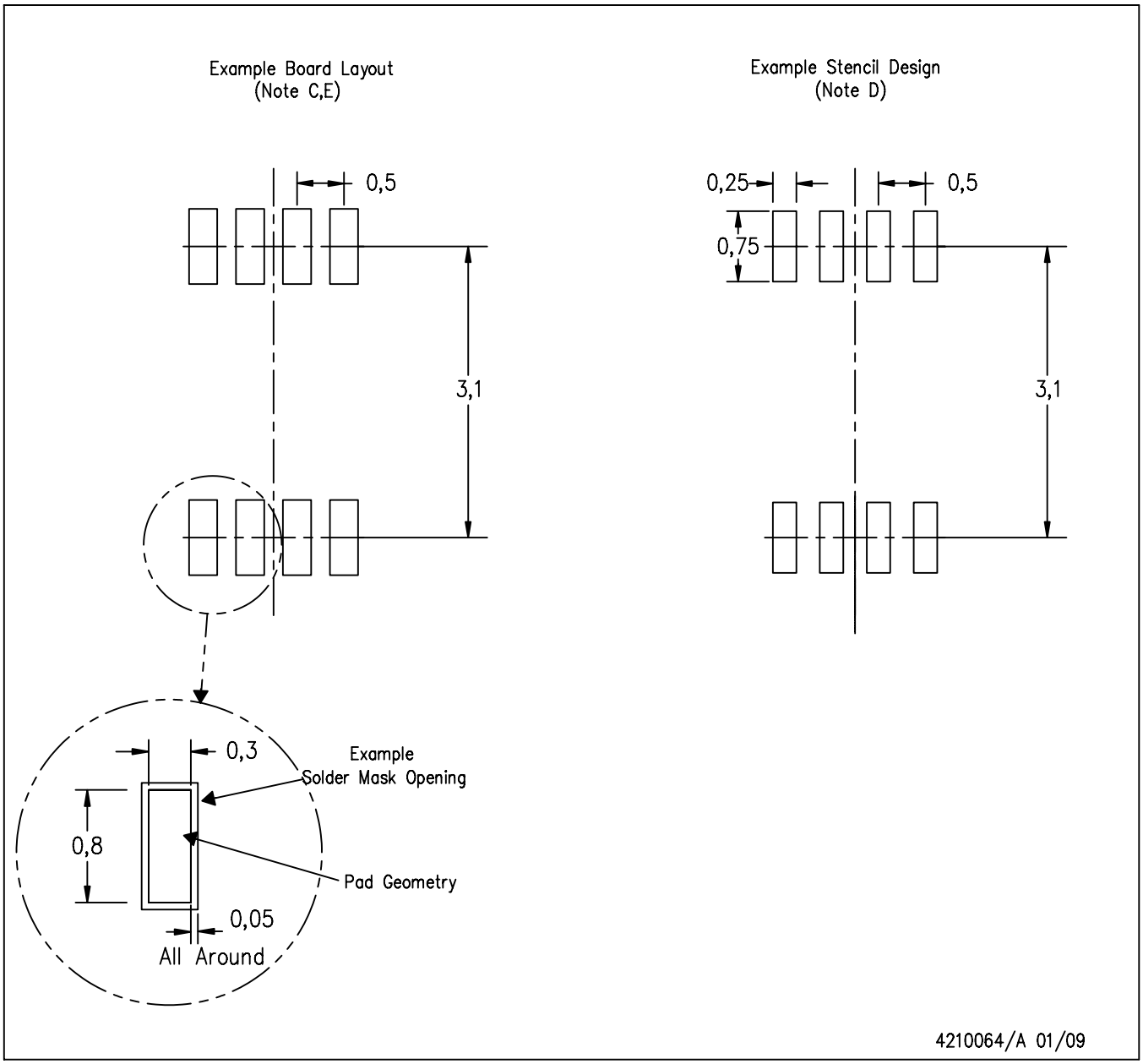
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S-PDSO-G8)



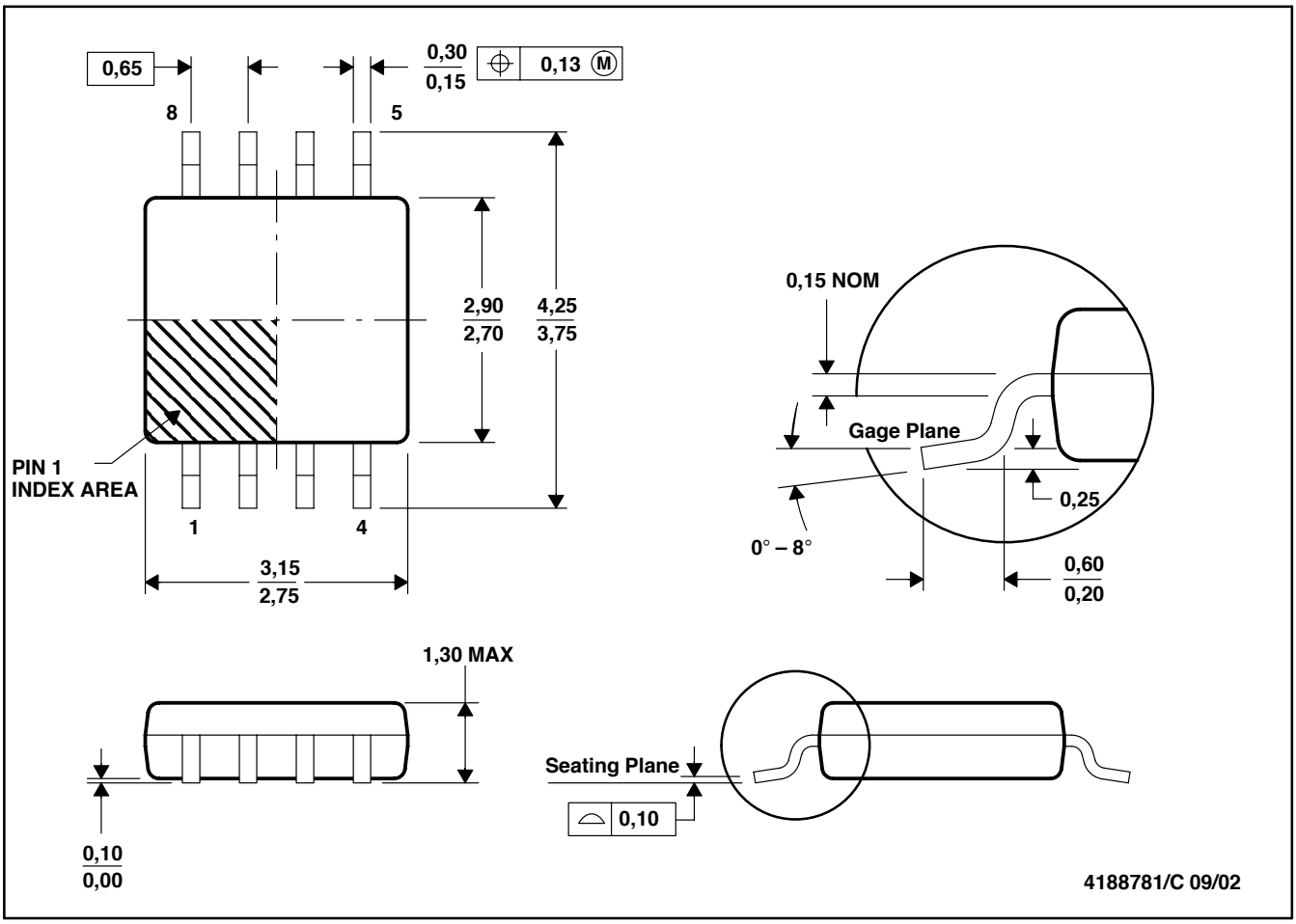
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (S-PDSO-G8)



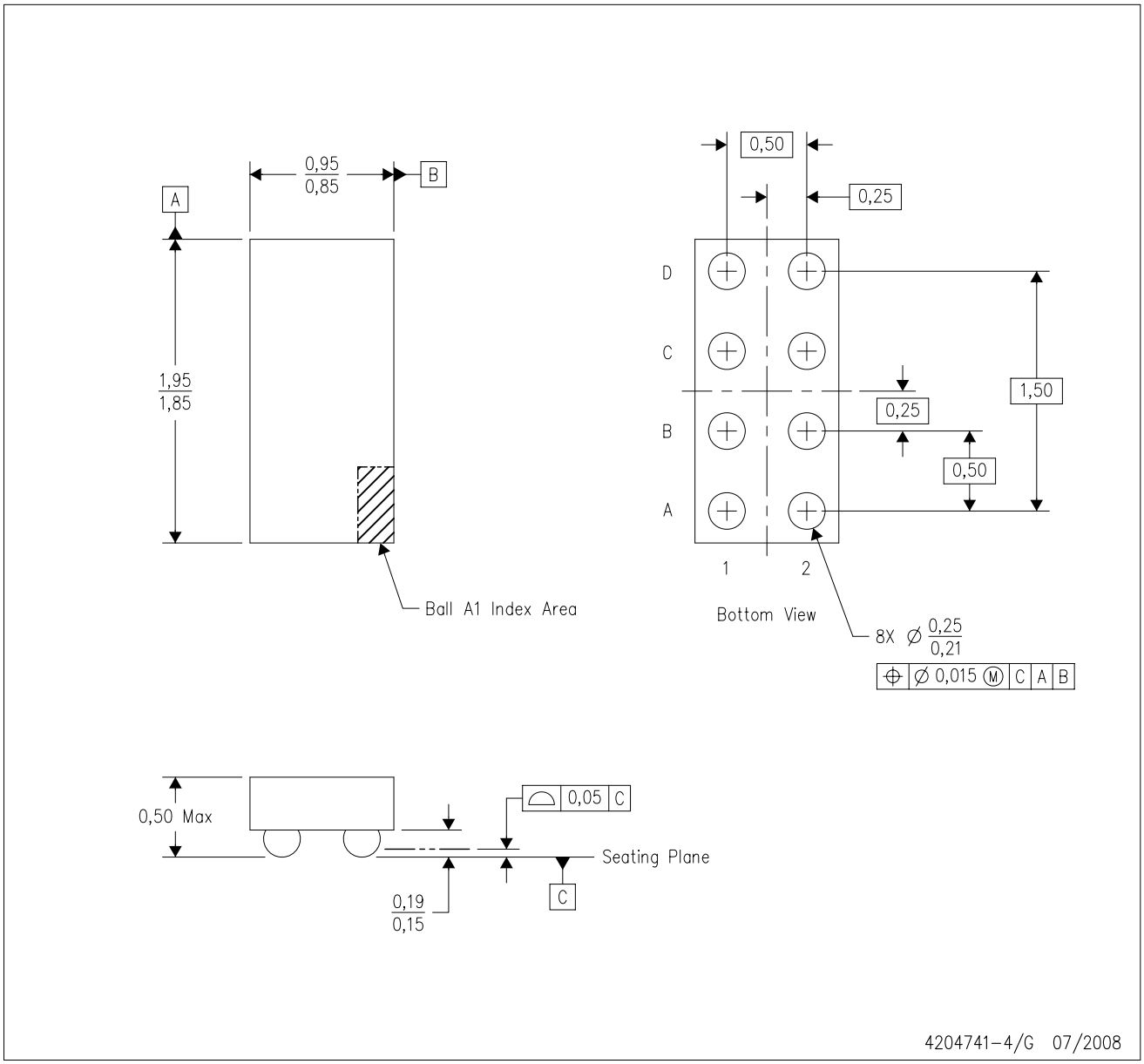
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

YZP (R-XBGA-N8) DIE-SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

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